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A MICROPROCESSOR BASED TELEMETRY OUTSTATION

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Cape Town

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By J. H. Lusty

ABSTRACT

This thesis describes the development of a microprocessor based telemetry outstation used to collect analogue and digital data at remote sites for the Cape Town City Council's Waterworks Branch of the City Engineer's Department.

It is a functional equivalent of existing vendor supplied outstations which are not microprocessor based ie they rely purely on hardware. It was necessary to develop these units in-house due mainly to cost considerations since the vendor supplied units were becoming increasingly expensive; furthermore, they are using obsolescent technology and the purchase of spare parts has become increasingly difficult. This latter situation has been aggravated in more recent times by the threat of sanctions. The expertise gained by the writer from the development phase has already been directly applicable to another telemetry project for the Cape Town City Council. This dramatically shortened the development time. Further projects of this nature are envisaged.

The outstation collects dam level and water flow rate values and alarms at remote sites, most of them reservoirs. In addition, the flow rates are integrated with respect to time to give volumes. These quantities are transmitted back to the master station via a modem and u.h.f. tranceiver when interrogated by a master station.

The development of the outstation involved a detailed analysis of the telemetry protocol between the master station and five existing outstations. A complete set of general purpose hardware modules had to be designed with future applications in mind, a software philosophy formulated, implemented and tested and extensive field testing and evaluation performed before production of sixteen units commenced.

All the development work was done in the Computer Section of the City Electrical Engineer's Department in Cape Town.

DECLARATION

I declare that this thesis is my own, unaided work. It is being submitted in partial fullfilment of the requirements for the degree of Master of Science in Electrical Engineering to the University of Cape Town. It has not been submitted before for any degree or examination at this or any other university.

John Hilary Lusty
(Name of candidate)

Signed by candidate

Signature Removed

22nd day of September 1986.

PREFACE

The writer originally became involved with the Cape Town Municipal water telemetry system when the master station, a GEC 2050 mimi-computer was upgraded to accomodate twenty-one outstations from an original five. At this stage, the Municipality had not purchased the additional outstations, and since these were becoming increasingly expensive and were using dated technology, the writer was asked to investigate the feasability of developing an economic microprocessor based look-alike unit.

After a preliminary investigation, it was found that the necessary hardware and software could be developed. The main problem which confronted the writer at this early stage was the lack of complete information regarding the telemetry protocols and data formats. Vendor supplied manuals were available but only explained the system in broad outline; all of the details had to be gleaned from actual measurements and observations on the working system.

The writer would like to acknowledge the very fruitfull discussions with his friend and colleague, Mr J vd S de Villiers, Senior Technician at the Computer Section of the Electricity Department's Test and Metering Branch, in which many conceptual ideas were shared from an early stage right through to prototype testing and production of the sixteen units. Also worthy of mention are Mr Kevin Frost, Senior Engineering Assistant, for the printed circuit layouts of the hardware, and the Departmental Drawing Office staff for the production of the Computer Aided Design circuit diagrams.

Finally, the writer would like to convey his sincere thanks to the City Electrical Engineer for permission to submit this thesis from development work done while in full-time employment of the Cape Town Municipality.

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CHAPTER 1 WHY TELEMETRY?

1.1 Introduction

The Cape Town Municipality provides the many essential services for the city itself and its environs. The supply and distribution of water for domestic and industrial use are but one of these.

With the passing of time, a distribution system expands and becomes a network with an ever increasing number of interrelated variables. When this happens, it becomes important to know what the various parameters are at a particular instant so that decisions can be made regarding the control of that network. When it is considered that Cape Town's water supply network consists of some nine dams, fifteen service reservoirs, fifteen pump stations, eight water treatment installations and approximately 30 000 Km of pipeline delivering 500 Ml/day, this becomes particularly true. The need for control is high-lighted under emergency conditions such as the recent pipe-burst on the Mitchell's Plein pipeline in July 1986. Timeous information is needed at a central point so corrective action may be taken. Refer to Fig 1.1 for a quasi-geographical layout of the Cape Town water supply network.

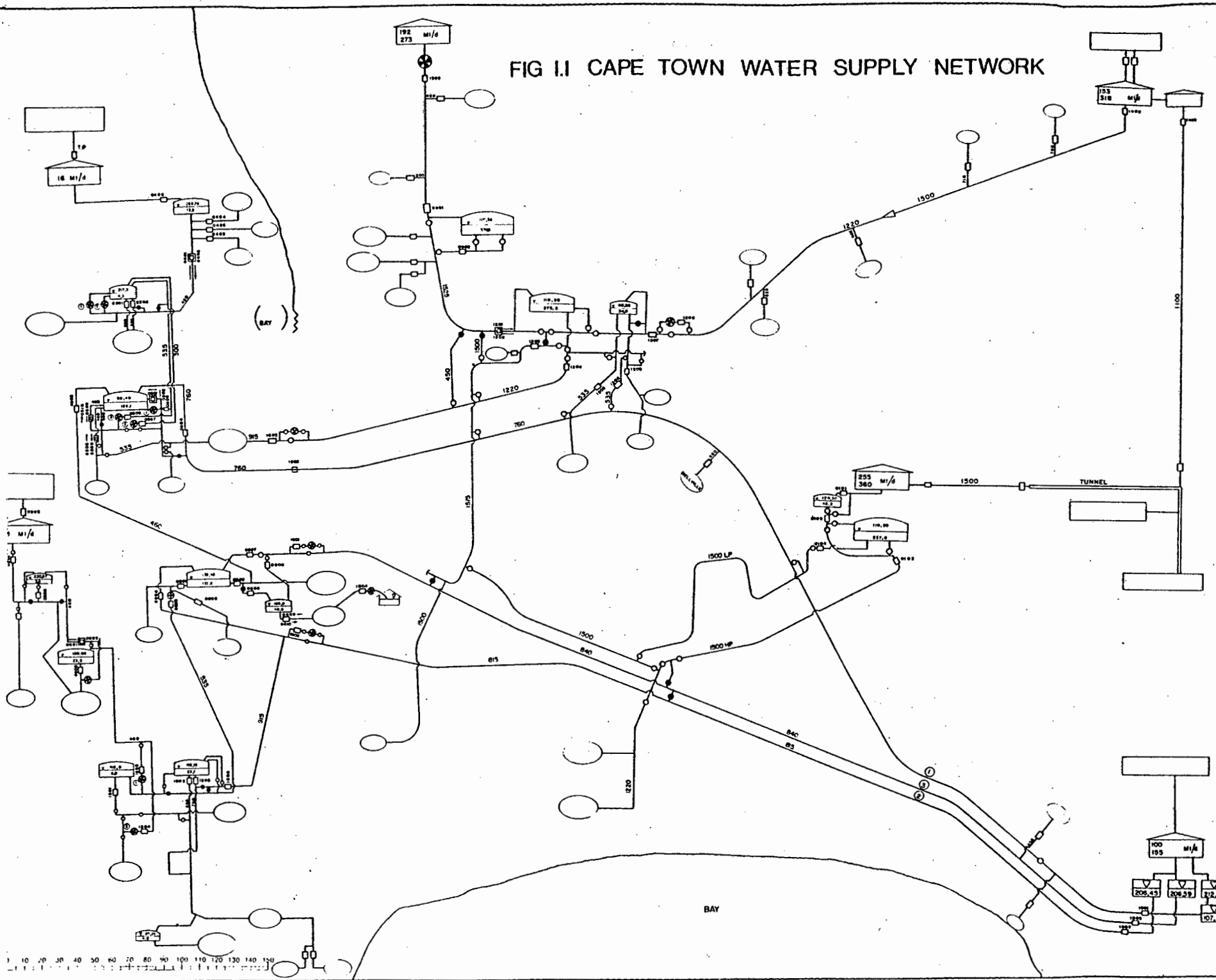
Control is not the only motivation for telemetry; statistical information gives vital information concerning consumption in various parts of the network. Planners need this to make pertinent decisions and intelligent estimates for future expansion. This in turn increases the telemetry requirements and so we have an ever increasing need for telemetry.

1.2 The measurement problem

What are the specific parameters to be measured and where?

At each measurement site, water levels, incoming and outgoing water flow rates and alarms are to be monitored; the alarms are mainly high and low water level points. In addition to these, the flow rates are integrated with respect to time to establish integrated flow rate values ie actual volumes of water.

FIG I.1 CAPE TOWN WATER SUPPLY NETWORK



notes

FLOW METERS

TELE-METERED	METER CHAMBER	GAUGE PLATE	DETAILS
			SAND VALVE TREATMENT PLANT OUTLET R.C. OUTLET SAND VALVE RAW WATER INLET
			RESERVOIR TREATMENT PLANT OUTLET R.C. OUTLET RAW WATER INLET TO T.P.
			RESERVOIR OUTLET OUTLET
			RESERVOIR INLET OUTLET INLET RAW WATER INLET TO T.P.
			RESERVOIR INFLOW INFLOW INFLOW INFLOW INLET OUTLET INLET TO RETICULATION OUTLET TO RETICULATION INLET TO RETICULATION OUTLET TO RETICULATION
			RESERVOIR INLET OUTLET TO PUMP & METER
			RESERVOIR OUTLET OUTLET OUTLET OUTLET TO RETICULATION OUTLET TO RES. NO 2 OR RES. INLET NO 1 INLET NO 2 OUTLET TO RETICULATION OUTLET TO RESERVOIR
			RESERVOIR FLOW ZERO FLOW TO RESERVOIR
			FLOW FLOW
			RESERVOIR INFLOW OUTFLOW INFLOW OUTFLOW
			RAW WATER INLET OUTLET
			RAW WATER OUTLET R.C.
			RESERVOIR OUTFLOW OUTFLOW INFLOW OUTFLOW INLET OUTLET
FIELD FLOWS			
			PUMP STATION PUMP PORTION INLET OUTLET

TREATMENT PLANTS — RESERVOIRS

2	85 04	D.G.R	AMENDED
1	83-11-15	R.S.S	Granted

CITY OF CAPE TOWN
CITY ENGINEER'S DEPT.

J.G. BRAND city engineer

branch head

project title: SCHEMATIC DIAGRAM

drawing title: BULK MAINS AND METERS

scale	drawing no.
N.T.S.	revision suffix
date DEC 81	drawn D.G.R / traced P.W.J / checked

The level transducers may be analogue or digital, the flow rate transducers are analogue and the alarms are digital. The integrated flow rates are derived from the flow rate parameters on site.

Thus there is a variety of analogue and digital data quantities to be measured at each site and gathered by the outstation. The analogue parameters are to be converted to digital form. All parameters now being digital are to be transformed into a suitable format for transmission via a modem.

In addition to analogue and digital input information from the outstation, digital output information may be transmitted from the master station to the outstation. This is hereafter referred to as status output information and in the existing system is used to switch two remote loggers on and off and to control mechanical flow rate integrators. This is not required for the additional outstations since no further loggers are required and the integrated flow rates are to be derived from the flow rates by the outstation software.

Digital data lends itself very readily to transmission via modems using simple frequency-shift-keying (FSK) techniques since it suffers no loss of accuracy in the transmission path when easily utilised error detection codes are embedded in the messages. This would not be possible using analogue transmission methods.

All the measuring sites are remote, in some cases over 100 Km from where the data is required. For this reason, transmission from the outstations to the master station is done by u.h.f. radio, since landline would not be viable. Several problems arise from this which will be described in detail.

Up to twenty-one outstations are envisaged in the near future. The measurement problem may therefore be formalised as the transmission of a variety of analogue and digital data from each of twenty-one remote outstations back to a central master station using modems and radios.

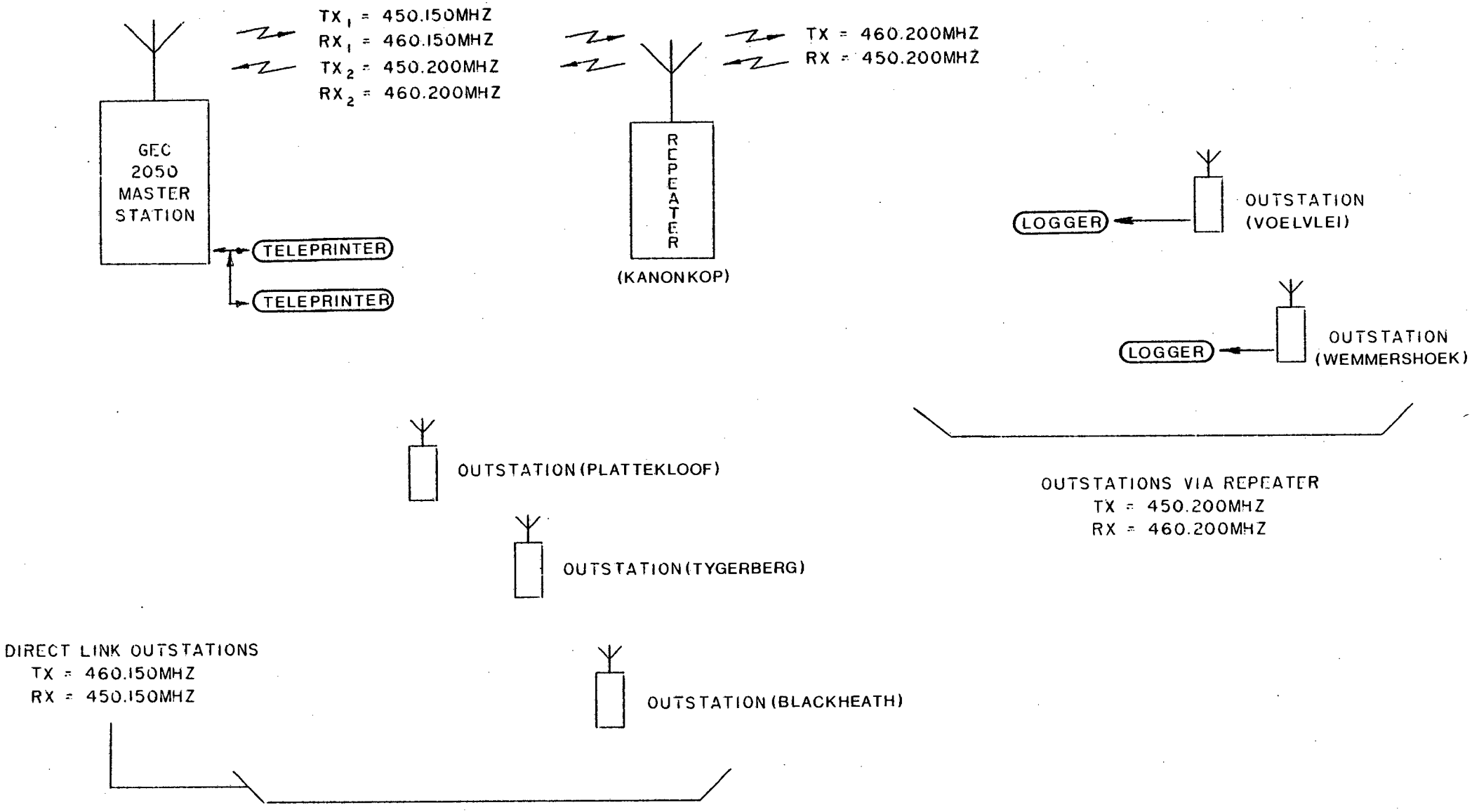
1.3 The existing system

Before the writer became involved in this project, the Waterworks Telemetry System consisted of a GEC 2050 mini-computer as a central master station and five GEC TELEPACE outstations at Voelvlei, Wemmershoek, Plattekloof, Tygerberg and Blackheath. The master station is situated at the Test and Metering Branch of the City Electrical Engineer's Department and is connected to two teleprinters, a local one at the master station and a remote one at Albion Springs, the main depot of the Waterworks Branch. The two teleprinters operate in parallel and are used for the printing of logs at regular intervals ie timed logs, for the printing of on-demand logs and for parameterisation of the system e.g. allowing or inhibiting a particular outstation, determining how often timed logs are printed, and the setting of limit values for dam levels. If these limit values are exceeded, or an alarm occurs at an outstation site, spontaneous alarms are printed on the teleprinters.

There are two further logging printers at Voelvlei and Wemmershoek which are output-only devices which print the same timed logs as the master station teleprinters. There is also a spontaneous log printed on the teleprinters once a day at 8.00 am.

Timed logs contain level and flow rate values for all the outstations which are allowed, on-demand logs contain level and flow rate values for the outstation requested and the spontaneous once-per-day log contains the integrated flow rate values for all outstations which are allowed. Immediately after the printing of this spontaneous log, the mechanical integrators are reset using a sequence of status output messages. This is described in more detail in paragraph 1.5.3.4. It is at these two remote logging sites, Voelvlei and Wemmershoek that the level and flow rate information contained in the timed logs is most needed. Refer to Fig 1.2 for an overall schematic diagram of the system.

Appendix A gives examples of the different types of logs described here.



EXISTING TELEMETRY SYSTEM

FIG 1.2

There are actually two radio communication channels operated in parallel; one is a direct path from the master station to Tygerberg, Plattekloof and Blackheath and the other via a u.h.f. repeater located at Kanonkop. This second channel via repeater is necessary for the Voelvlei and Wemmershoek outstations due to their location.

1.4 Inadequacies of the existing system

Due to the increasing need for telemetry on the Waterworks system, the origonal five TELEPACE outstations were proving inadequate. For this reason the master station software was expanded using vendor supplied software to accomodate an additional sixteen outstations making the total of twenty-one, the figure previously mentioned in paragraph 1.2.
At this time, the cost of the TELEPACE outstations had risen appreciably and they were becoming increasingly obsolescent in the technology used. This posed an additional problem of eventual non-availability of spare parts. After conducting a brief feasability study, the writer felt that a microprocessor based unit could be produced which would in every way emulate the older hardware-based TELEPACE units. Not only would this be cost effective since sixteen units would be produced, but much valuable experience would be gleaned and would be applicable to future telemetry projects.

1.5 Communications protocol

In order to draw up a formal specification for the proposed TELEPACE look-alike, a detailed analysis of the existing system's communication protocol was necessary. Unfortunately, this is only documented in broad outline by the vendor and considerable time was spent in determining the exact parameters by careful measurements taken on the system while it was operating. These are now precisely formalised.

1.5.1 Modem channel

This is a 600 Baud FSK channel in the audio frequency band using two frequencies of 1300Hz and 1700Hz; note that no central carrier frequency as such is ever transmitted ie there is either a tone of 1300Hz or 1700Hz or no tone at all. The mode of communication is half-duplex ie both master station and outstation transmit and receive on the same channel but not at the same time.

1.5.2 Message protocol

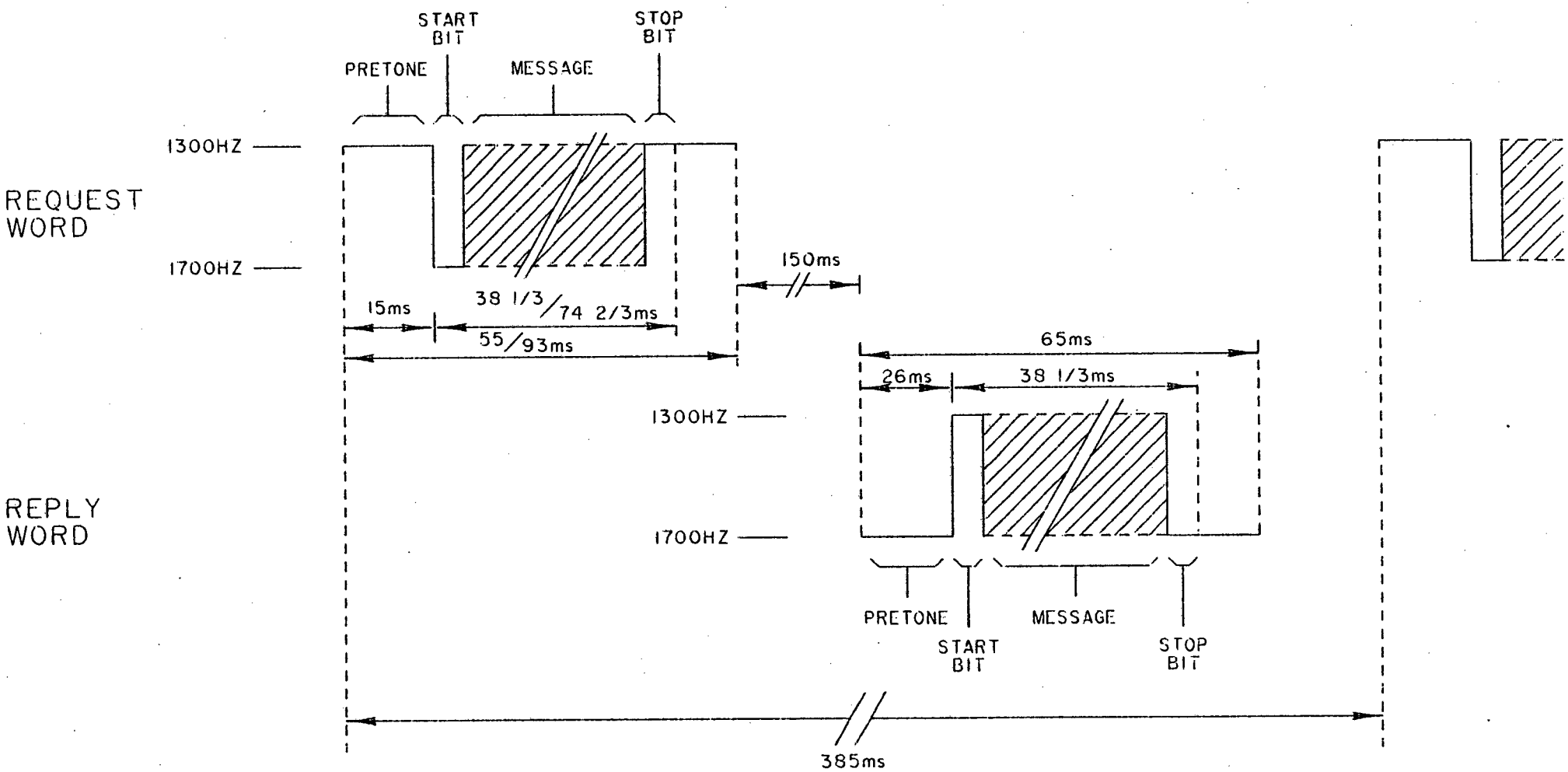
Fig 1.3 indicates the request word/reply word protocol under normal conditions. The timing parameters shown are exact only for the start bit/stop bit/message periods; these are well defined and may be calculated from the baud rate and message bit lengths. The other timing parameters shown are usually not critical and are therefore approximate; these are actually measured on the working system. The following points are important:-

(i) Polling frequency is normally 1000/385 Hz ie just under 3Hz.

(ii) A period of pretone precedes both the request and reply words; this is to allow the demodulators at the master station and the outstations to lock onto the incoming VFT (voice frequency transmission) signals.

(iii) Start bit and stop bits are of opposite polarity and of opposite sense for the request and reply words. This is also related to the fact that for the request word, the VFT signal commences at 1300Hz, changes to 1700Hz for the start bit and terminates at 1300Hz at the end of the transmission; the opposite is the case for the reply word. In this way, the direction of information transmission can be established by the sense of the start and stop bits.

(iv) The elapsed time between the end of a request word and the beginning of a reply word is approximately 150ms; this is not critical and may vary in some cases. All that really matters is that the master station receives a reply word before commencement of the next request word.



REQUEST/REPLY WORD PROTOCOL

FIG 1.3

(v) In the request word, two of the timing parameters have two possible values; this is because request words may be either single or double messages. This is explained fully in paragraph 1.5.3.

(vi) If a reply word from an outstation is invalid, the master station asks for this point up to five times at a slower polling rate of +/- 1 Hz; if a satisfactory reply is not received, the point failure is logged at the master station and that point is only polled once in subsequent polling cycles until a valid reply is received; when this occurs, the reinstatement of that point is logged and the slow polling of up to five times on subsequent failure is restored.

1.5.3 Message format

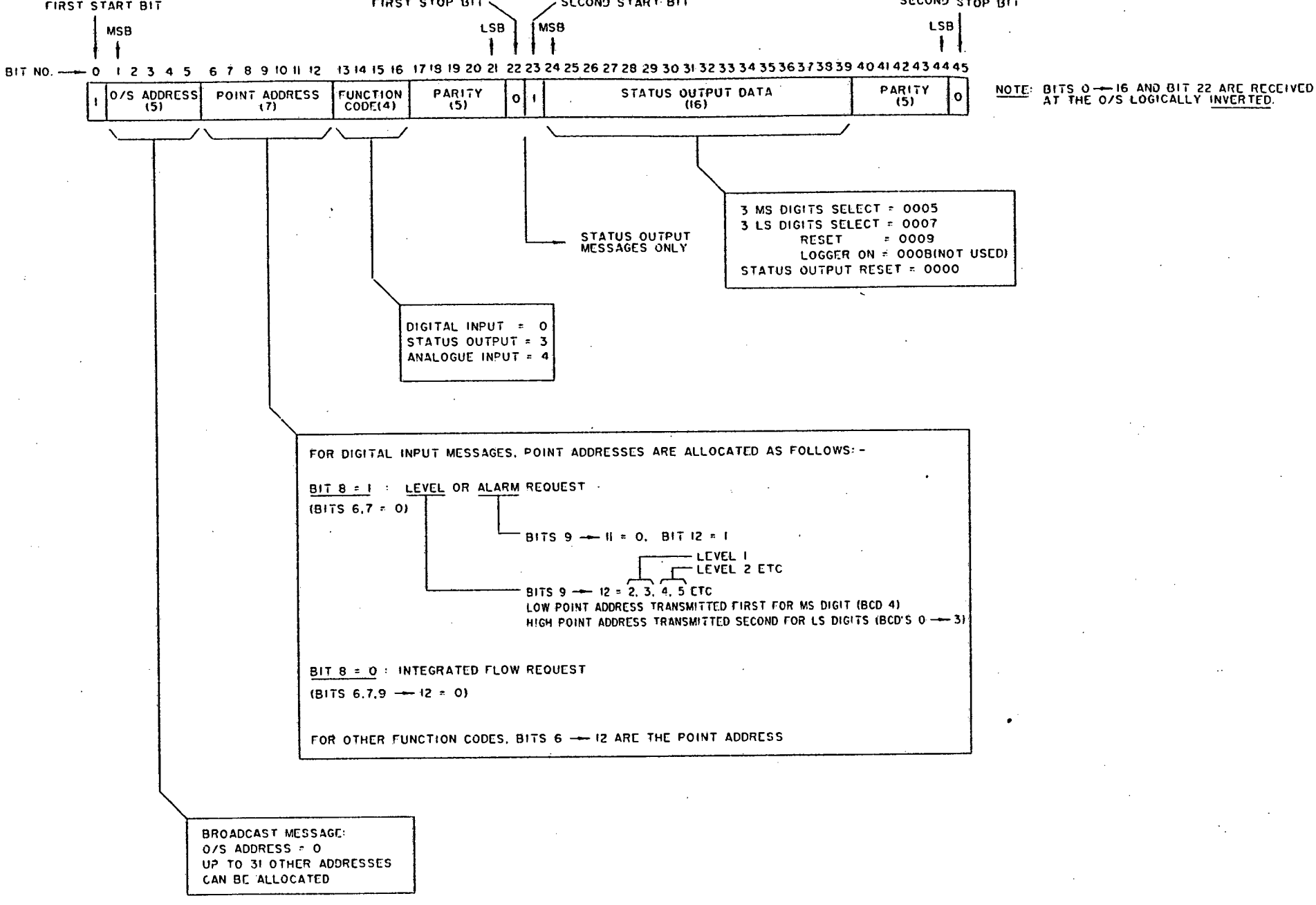
Refer to Fig 1.4 for request word data format.

The request words from the master station are either single messages for digital and analogue input or double messages for status outputs.

Single messages are 23 bits long, consisting of a start bit, 5 outstation address bits, 7 point address bits, 4 function code bits, 5 parity bits and a stop bit. Double messages are 46 bits long, the first half having the same format as a single message, and the second half consisting of another start bit, 16 data bits, 5 parity bits and another stop bit. The parity bits are generated by dividing the data polynomial by $1 + x^2 + x^5$. Refer to Appendix B for a complete treatment of the parity generation. It should be noted that the start bit and the following 16 bits are logically inverted BEFORE the parity bits are generated, and that the stop bit plays no part in the parity generation. This is most important since the process of inversion and parity generation are not in general commutative ie the order of operations does matter. Bit 0 (the start bit) is the most significant bit and is transmitted first, followed by the remaining bits.

Analogue input messages are used for flow rates, digital input messages are used for levels and alarms when bit 8 in the point address is 1 and integrated flow rates when this bit is 0, and status output messages are used to select either the three most or least significant digits of an integrated flow rate or to switch the remote loggers at Voelvlei and Wemmershoek on and off. This is described more fully in paragraph 1.5.3.4

Reply words are always single messages and consist of a start bit, 16 data bits, 5 parity bits and a stop bit. The parity bits are generated in the same way as for request words, but the start and stop bits are of opposite sense as request words. (request words have start bit = 0, stop bit = 1; reply words have start bit = 1, stop bit = 0). It should be noted once again that the start bit (which is now inverted for reply words) plays a part in the parity



REQUEST WORD DATA FORMAT | FIG 1.4

generation and hence this inversion affects the parity bits. As for request words, reply words are transmitted start bit first (bit 0, the most significant bit), followed by bits 1 to 22.

Refer to Fig 1.5 for the reply word data format which shows bits 1 to 16 of the reply word for each type of point written into the packed data word MESP by the software (refer paragraph 4.4).

1.5.3.1 Alarms

Up to ten alarms can be transmitted using bits 1 to 10; bits 11 to 16 are unused and must be set to 0 (ie not don't cares), otherwise the master station halts a little while later. Unfortunately, due to the 'black box' nature of the master station as a whole, the reason for this is unknown. The writer suspects a software bug in the master station software but is not able to find it as it is not documented in sufficient detail. If an alarm bit changes state from 1 to 0 then that is an alarm condition and is logged as a failure on the master station teleprinters; if a bit changes state from 0 to 1 then this is a removal of an alarm condition and is logged as an OK condition.

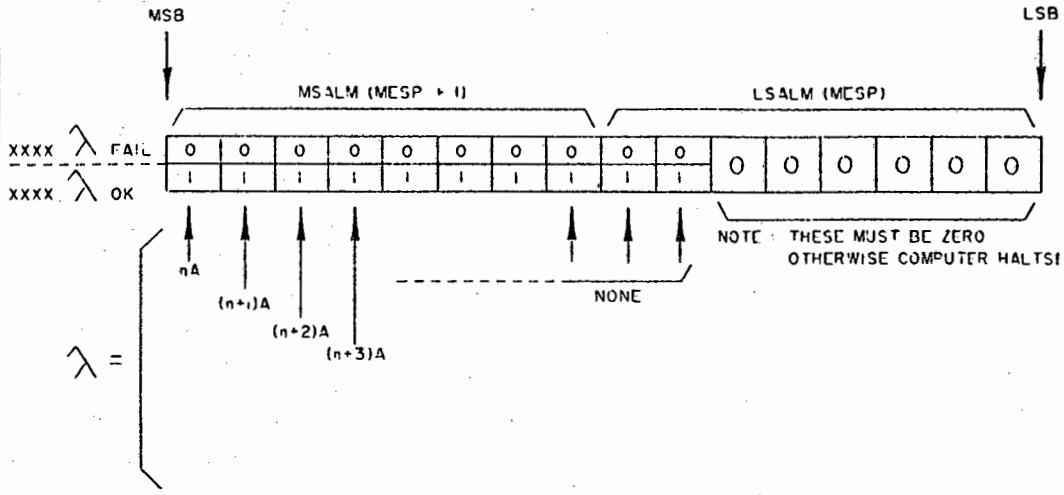
1.5.3.2 Levels

Each level is a 5-digit BCD value and therefore requires two request word/reply word sequences. Note that the BCD digits are inverted and that in the first reply, only the most significant digit BCD4 is transmitted, the other three unused nibbles being set to F, followed by a second reply word containing the remaining BCD digits 0 to 3. Note the two 23-bit reply words of a level should not be confused with the 46-bit double message request word for status outputs.

1.5.3.3 Flow rates

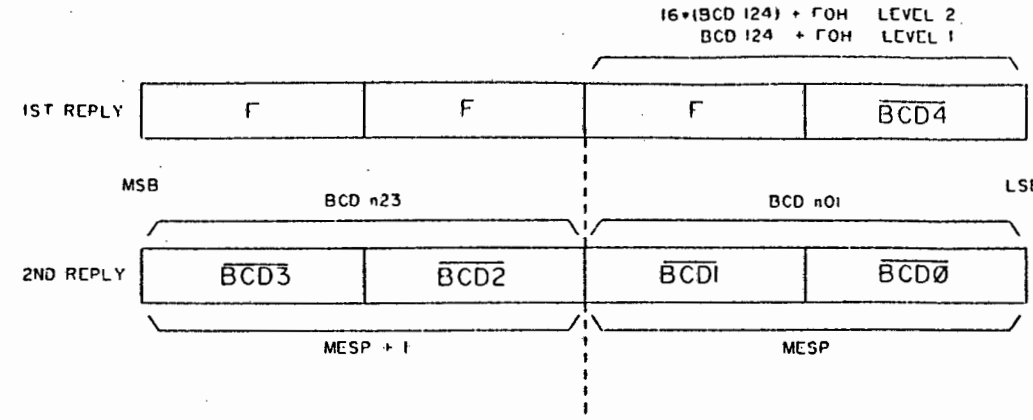
Flow rates are 3-digit BCD values and are non-inverted. The high order nibble in MESP+1 is a don't care.

ALARMS



PRINTOUT FORMAT : XXXX (n+k)A FAIL
XXXX (n+k)A OK
WHERE n = HIGHEST POINT NUMBER + 1.
k = 0 TO L-1 WHERE L = NO. OF ALARM POINTS AT OUTSTATION XXXX

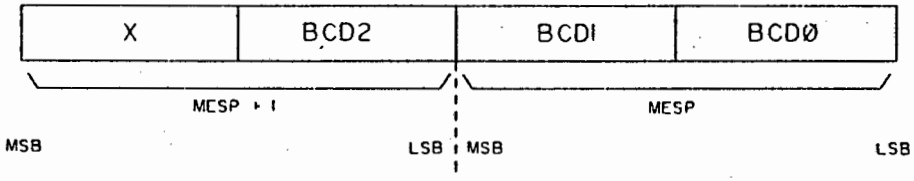
LEVELS



LEVEL 1, n = 1
LEVEL 2, n = 2
— FOR DIGITAL LEVELS ONLY

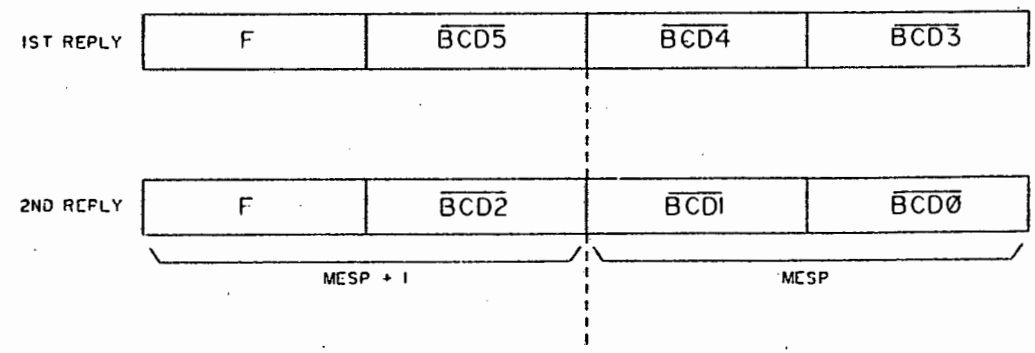
PRINTOUT FORMAT : BCD4 BCD3, BCD2 BCD1 BCD0 M

FLOW RATES



PRINTOUT FORMAT : BCD2 BCD1 BCD0 ML/D (FOR MULTIPLIER AND DIVISOR SCALE FACTORS = 1 OFFSET = 0)

INTEGRATED FLOW RATES



PRINTOUT FORMAT : BCD5 BCD4 BCD3, BCD2 ML (BCD1 AND BCD0 IGNORED)

REPLY WORD DATA FORMAT (REFER APPENDIX A) FIG 1.5

1.5.3.4 Integrated flow rates

Integrated flow rates are 6-digit BCD values and therefore, like levels, require two request word/reply word sequences each. The BCD digits are inverted and the three most significant BCD digits 3 to 5 are transmitted first, followed by the three least significant BCD digits 0 to 2. In both reply words, the most significant nibble is set to F. Note that BCD0 and 1 are not actually logged but ignored altogether.

In all the above data types, the printout format referred to in Fig 1.5 is as the information is printed out on the master station teleprinters. Refer to Appendix A for further information concerning printout formats.

In the normal polling cycle of the outstations by the master station, all the points of a particular outstation are polled and then the next outstation is polled and so on. The sequence of polling the points at a particular outstation is not normally relevant since each request word requires a unique reply. This is not quite true for status output polling which follows a set sequence due to the nature of the hardware at the remote TELEPACE sites to which they pertain.

Each time an integrated flow rate is required from the outstation (once a day for the 8.00 am spontaneous log described in paragraph 1.3) the sequence of polling is:-

(i) Integrated flow rate meter MS BCD digits select (status output double message request word).

(ii) Integrated flow rate meter MS BCD digits read (digital input single message request word).

(iii) Integrated flow rate meter LS BCD digits select (status output double message request word).

(iv) Integrated flow rate meter LS BCD digits read (digital input single message request word).

(v) Integrated flow rate meter reset (status output double message request word).

(vi) Integrated flow rate meter back to normal operation (status output double message request word).

The reason for this sequence is that at the sites where TELEPACE outstations are installed and integrated flow rates are read, the flow rate integration is done mechanically. This mechanical integrator has an electronic multiplexer. A TELEPACE status output card is connected to a set of control lines which selects either the most or least significant three digits of an integrated flow rate which can then be read by a TELEPACE digital input card. These status output control lines are also used to reset the integrator. Hence the requirement for the sequence of interleaving status output and digital input request words. In the microprocessor based units the mechanical integrators will be dispensed with and the integration done with software. This is dealt with in full in Appendices F and H.

Status output request words are also used for switching the remote loggers at Voelvlei and Wemmershoek on and off for the timed logs mentioned in paragraph 1.3; this facility is not required in the new microprocessor based outstations but could be added later if required.

Whenever a status output request word is sent, an all-zero confirmation word is sent as a reply.

1.6 Formal specification

Paragraph 1.5 formally specifies all the parameters necessary for the proposed microprocessor based look-alike outstations to emulate the existing GEC TELEPACE outstations. In addition to the above, the following were considered desirable:-

(i) The hardware should be as modular as possible. This makes maintenance quick and easy and the modules interchangeable between outstations. Furthermore, future telemetry projects were borne in mind so that benefit could be derived from the writer's design efforts at a later date. This policy has already paid off handsome dividends in the production of a subsequent telemetry system viz. the Robben Island Radiation Monitor.

(ii) The unit should be as compact as possible. The older TELEPACE units are bulky and use large printed circuit boards with many small-scale integrated circuits. Advantage should be taken of the much larger-scale integrated devices currently available.

(iii) The unit should be as 'soft' as possible. What is meant by this is that since the unit is microprocessor based and therefore software controlled, make the software do as much of the task as possible ie minimise the hardware and maximise the software task. The space and cost of a little more EPROM in a system is insignificant when hardware design time, production and testing is considered. This concept of 'soft' systems is now a well established trend in computer based equipment.

(iv) Having adopted the 'soft' policy of (iii), the modular policy of (i) can be applied to the software too. This should be broken down into a number of functionally well defined software modules. As with the hardware modules, most of the software modules required little or no modification to produce the Robben Island Radiation Monitor Outstation. In fact, the writer completed the software for the above-mentioned system in twelve hours because almost all the work had been done during the thesis research period! Furthermore, some of the software modules were also used in the Robben Island Radiation Monitor Master Station.

Thus the writer's modular strategy has already proved itself in preserving his employer's design investment for future telemetry projects.

(v) The unit should be mains powered. Battery backup was considered but would have been pointless as far as the levels and flow rate transducers are concerned since they are also mains powered. However, in the event of mains power failure it should be realised that the integrated flow rate values would be lost for that day since they are to be done with software as mentioned in paragraphs 1.2 and 1.5.3.4. This is not too serious since power-failures are fairly rare.

CHAPTER 2 HOW DO WE APPROACH THE PROBLEM?

2.1 Introduction

Having formalised the specification for the telemetry outstation in Chapter 1, three main aspects emerge. These are:-

(i) Telemetry communications.
(ii) External data input.
(iii) Internal data processing.

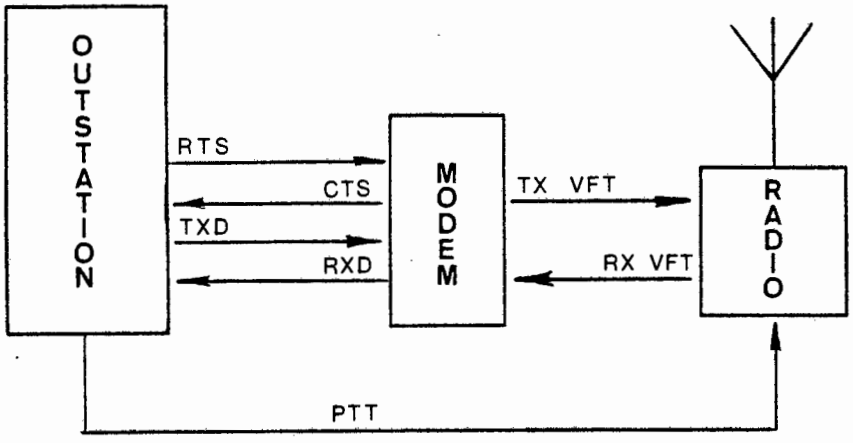
These areas are all somewhat interrelated and many of the tasks could have been achieved in more than one way. The purpose of this chapter, therefore, is to explain how the problems which arise in the specification were approached and whether they should be done in software, hardware, or a combination of both. Once finalised, this forms the basis of subsequent chapters where full details will be given.

2.2 Telemetry communications

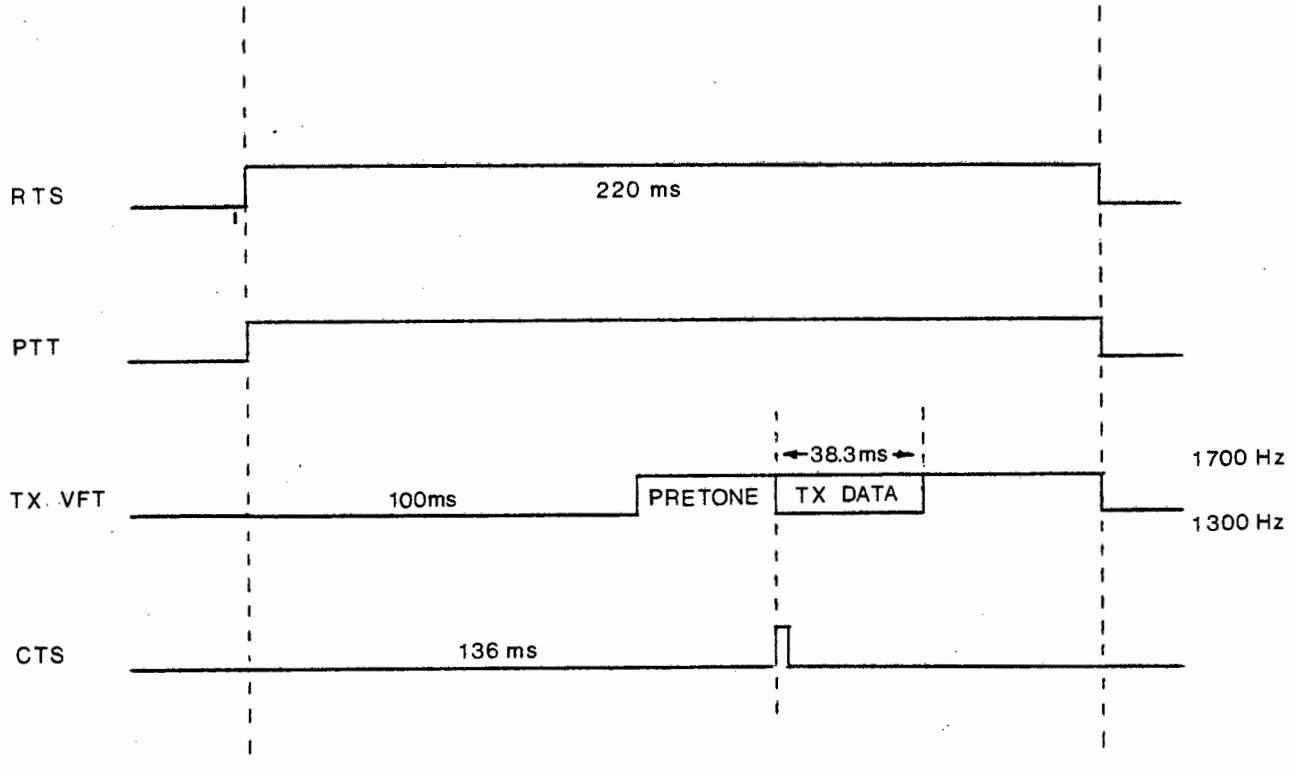
These were discussed in some detail in paragraph 1.5. The channel, the protocol and the message format are already defined.

The outstation has to receive request words asynchronously ie at any time regardless of what it may be doing, and transmit reply words back to the master station in accordance with Fig 1.3. It has to control a modem and a u.h.f. transmitter, taking into account the warm-up time it requires. The outstation issues a request-to-send (RTS) signal to the modem and a press-to-talk (PTT) signal to the radio, thereby keying the transmitter. Allowing for TX warm-up time of the u.h.f. transmitter, the modem then issues a clear-to-send (CTS) signal to the outstation which then transmits the reply word. Refer to Fig 2.1 for a block diagram of this handshaking. The u.h.f. transmitter TX warm-up time can be anywhere between 50ms and 150ms . For the particular radios used, 100ms was quite adequate. Bearing these two facts in mind, the outstation reply timing diagram may be derived; this is shown in Fig 2.2.

This should be compared with Fig 1.3, where the measured reply timing parameters of the existing TELEPACE outstations are shown. Note the following differences between the two:-



BLOCK DIAGRAM OF RADIO/MODEM CONTROL | FIG 2.1



REPLY TIMING DIAGRAM | FIG 2.2

(i) The TELEPACE modem pretone period is 26ms; this is not critical so a design figure of 36ms was used, leaving a generous 10ms margin.

(ii) The TELEPACE outstations switch off the modem VFT signal almost immediately after the stop bit ie after

(65 - 26 - 38.3) ms = 0.7 ms

whereas the microprocessor outstations switch off after

(220 - 136 - 38.3) ms = 45.7 ms

The differences in (i) and (ii) above are not important since they only affect non-critical parameters as mentioned in paragraph 1.5.2.

It was decided to design an in-house modem which would not only satisfy the channel requirements of 600 Baud and 1300Hz/1700Hz but also the protocol timing requirements. In accordance with paragraph 1.6 (iii) it should be as 'soft' as possible ie the timing parameters and the control to be done by software.

This hardware module if hereafter referred to as the MODEM module.

The request word has to be clocked into and the reply word has to be clocked out of the outstation asynchronously. If the messages had been 8-bit words plus a simple odd/even parity scheme, this might have been a case supporting a conventional ACIA (Asynchronous Communications Interface Adapter) such as the MOTOROLA 6850 or INTEL 8251; however, due to the 23-bit word length and the somewhat more complex parity scheme, this could not be done. A hardware approach was tried where a special piece of hardware was developed using random logic but it used approximately fifty integrated circuits! This was obviously not the way to go, and with a little investigation it was found that a software approach was quite feasable.

The decoding of the request words and encoding of the reply words is unquestionably a software task and is discussed in detail in paragraph 4.5.

2.3 External data input

These are the flow rates which are analogue, the levels which can be analogue or digital and the alarms which are digital. It was decided to design general purpose hardware modules to perform this task. They would be under software control.

The analogue-to-digital converter modules must have input circuits which are galvanically isolated from the microprocessor power supply of the outstation. This is considered necessary because the writer's experience with other projects has shown that the effect of commoning external transducers to the outstation supply can sometimes produce undesirable behaviour due to unplanned earth loops or other unforeseen conditions.

This hardware module is hereafter referred to as the A/D module.

The digital input modules are also galvanically isolated from the microprocessor supply. Again, a general purpose module is to be produced which would also have output capability ie an input/output module.

This hardware module is hereafter referred to as the I/O module.

2.4 Internal data processing

This can be broken down into two tasks ie numerical integration of the flow rate values with respect to time to obtain the integrated flow rate values, and data conversions.

2.4.1 Numerical integration

The flow rates are to be integrated with respect to time to give corresponding integrated flow rates for the 8.00 am print-out as discussed in paragraph 1.3. Since the master station polling is asynchronous as far as the outstations are concerned, the integrated flow rates have to be ready at all times; consequently the integration is an on-going process and must be done continuously. Since the integration is done numerically, this implies that each flow rate value must be summated at regular intervals to obtain a

running total from the last integrated flow rate reset message as discussed in paragraph 1.5.3.4, to the present time. This is done with software and is discussed in full in Appendix F.

2.4.2 Data conversions

The external data input parameters described in paragraph 2.3 all have to be converted by the software as follows:

2.4.2.1 Alarms

No processing is required for these except to ensure that the polarity and position of each bit is in accordance with paragraph 1.5.3.1

2.4.2.2 Levels

These are analogue quantities at the microprocessor based outstation sites (they are digital at the existing TELEPACE sites) and are therefore read from the A/D module. Refer to paragraph 3.2 for a fuller explanation of this. These raw level values have to be converted to 5-digit BCD in accordance with paragraph 1.5.3.2.

2.4.2.3 Flow rates

These are analogue quantities and are read from the A/D module. These raw flow rate values have to be converted to 3-digit BCD in accordance with paragraph 1.5.3.3

2.4.2.4 Integrated flow rates

These are internally generated quantities as explained in paragraph 2.4.1 and are derived from the raw flow rate values to obtain running totals; these running totals then have to be normalised by a 24-hour normalising factor and then converted to 6-digit BCD in accordance with paragraph 1.5.3.4. This is explained fully in Appendix H.

2.5 Outstation supervision

Having identified the three main aspects, a fourth one emerges viz. the overall supervision of the outstation hardware and software.

2.5.1 Software supervision

A multi-functioned hardware module was designed which has the following features:-

(i) A watchdog timer which is software parameterised ie a soft watchdog timer. Should the microprocessor for any reason jump off-program (usually caused by electromagnetic interference to the hardware), this soft watchdog timer ceases to be retriggered at regular intervals by the software and it automatically generates a restart pulse which is used to restart the entire outstation.

(ii) A regular pulse at one second intervals. This is used by the software to do the numerical integration of the flow rate values for the integrated flow rates as described in paragraph 2.4.1; the software also uses this to keep the soft watchdog timer retriggered.

(iii) Four 8-bit switch banks used to parameterise the outstation. These switches are read by the software and their exact use is discussed in paragraph 3.7.2.1.

(iv) Eight status indicator LED's which indicate which part of the software is being executed at any time. This is a valuable aid if the outstation malfunctions.

This hardware module is known as the parameters, watchdog and timer module, hereafter referred to as the PWT module.

2.5.2 Hardware supervision

A hardware module was designed with the following features:-

(i) A hardware watchdog timer with a much longer time-out period (approximately fifteen seconds) than the soft watchdog of the PWT module. This was added as a backup for the soft watchdog because the latter's behaviour relies on software parameterisation and therefore could conceivably become corrupted if the software malfunctions as described above. If this happens, the hard watchdog timer eventually times out and generates a repeated reset pulse at the time-out intervals mentioned above until the entire outstation is reset. This repetative behaviour until the outstation resets itself is useful for cases where the mains power has been restored after a break in supply, because sometimes the microprocessor does not automatically restart on power-up if the reset timing parameters are not satisfied; in these cases, the watchdog timer is useless since it is software parameterised during initialisation and the system will then rely on the well defined restart pulse from the hard watchdog timer.

Note that when the outstaton software is running normally, both the hard and soft watchdogs are triggered simultaneously.

(ii) Three LED's to indicate the integrity of the microprocessor power supply voltages. These voltages can also be measured on sockets.

This hardware module is known as the power indicator and watchdog timer module, hereafter referred to as the PWR module.

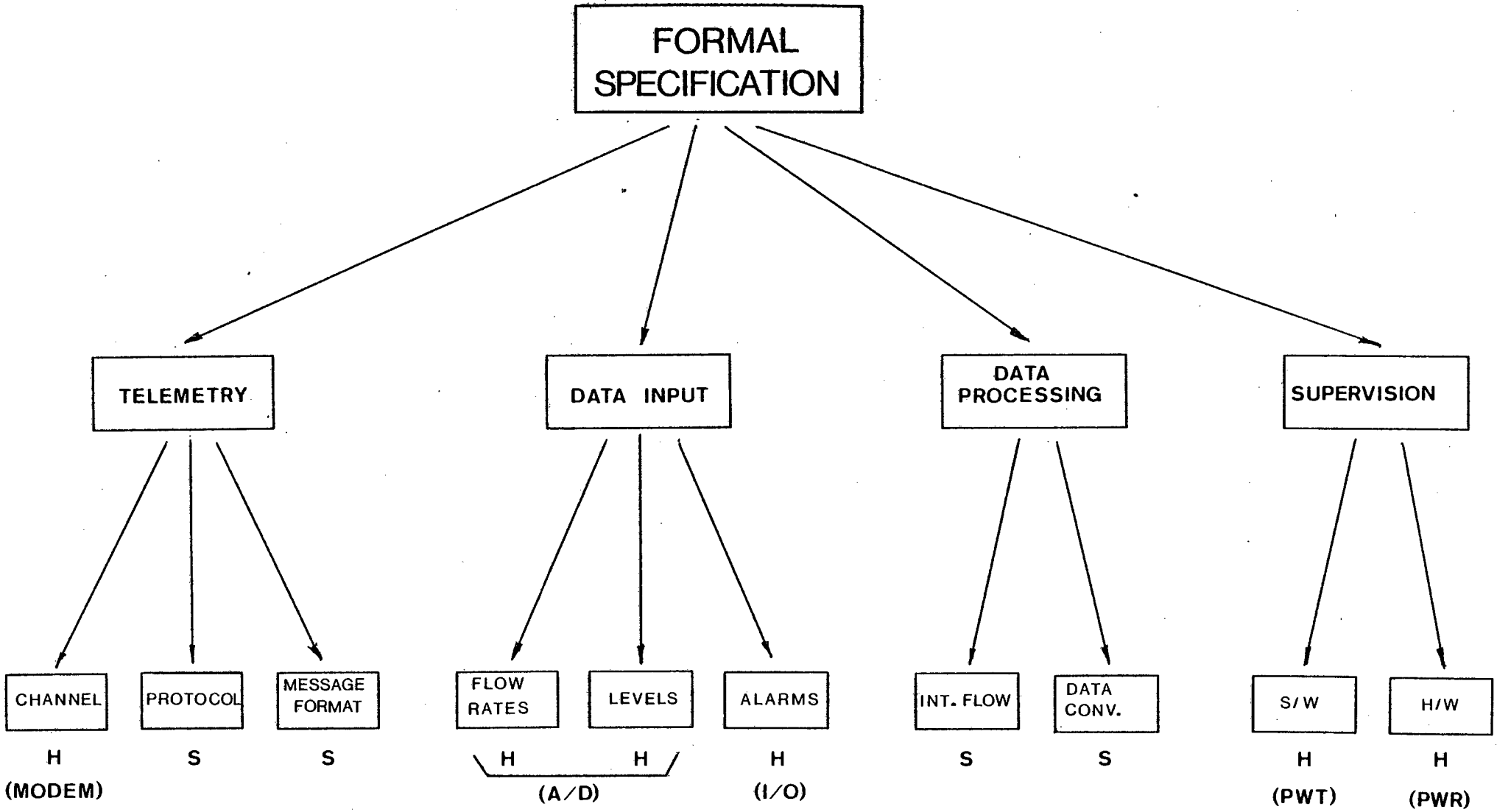
2.6 Summary

The breakdown of hardware and software tasks may now be summarised quite concisely with reference to Fig 2.3, where the elements of the formal specification of paragraphs 1.5 and 1.6 are broken down and assigned to hardware or software. Note that without actually having been stated so far, the presence of a Central Processing Unit for the software is obvious.

All the hardware modules are designed to interface with the S-64 SABUS. These are the MODEM, A/D, I/O, PWT and PWR modules which were designed for this project, but with general purpose applications in mind; they are indicated by the letter 'H' in Fig 2.3. The Central Processing Unit is a Single Board Computer, hereafter referred to as the SBC module. This is a vendor produced, of-the-shelf module, and is the only purchased module. It was pointless to design this as it is a standard unit.

All the software modules were written in assembler language for the INTEL 8085 microprocessor and are indicated by the letter 'S' in Fig 2.3; the 8085 was chosen since it is a well-tried proven industry standard.

Having identified all the software and hardware tasks, these are described in detail in subsequent chapters.



HARDWARE/SOFTWARE DIVISION

FIG 2.3

CHAPTER 3 THE OUTSTATION HARDWARE

3.1 Introduction

This chapter describes the SABUS hardware modules in detail, their specific functions, the design methods used to achieve these and how they are interconnected; this will pave the way for the software description that follows in Chapter 4. It should be noted beforehand that in designing these hardware modules, flexibility for future use in other systems was always in mind; consequently, the hardware often fulfills requirements over and above the immediate ones for this microprocessor based telemetry outstation. In some cases, the modules need to be configured according to the specific application; this will be explained.

3.2 System input requirements

The maximum requirements of any of the outstation sites are:-

2 levels
8 flow rates
3 integrated flow rates
10 alarms

At all of the existing TELEPACE and some of the new outstation sites, the level transducers are electromechanical with a 5-digit odometer-type display for a local readout. These transducers are fitted with a 5-decade BCD-encoded rotary switch interface which can be read by the outstation. To read this data from the switches requires 4 bits per decade ie 20 bits per level. At the new outstation sites, however, analogue level quantities are favoured since the digital level transducers will be phased out.

However, should an existing TELEPACE outstation be replaced with a new microprocessor based unit, the 5-decade digital level transducer should also be accomodated. In these cases, additional I/O modules can be fitted.

The above situation ie analogue or digital levels, has software implications which are explained in Appendix K. It also raises an accuracy/resolution question discussed in Appendix M.

Thus for an outstation reading analogue levels, the input requirements are 2 analogue channels for levels, 8 analogue channels for flow rates and 4 bits for alarms ie 10 analogue inputs and 4 digital inputs.

For an outstation reading digital levels, the input requirements are 8 analogue channels for flow rates, 40 bits for the two 5-decade BCD levels, and 4 bits for the alarms ie 8 analogue inputs and 44 digital inputs. The excessive amount of digital inputs in this case certainly favours the analogue level option.

Integrated flow rates are computed internally from the flow rates by the outstation software so there are no additional input requirements for these. This is explained fully in Chapter 4.

3.3 Hardware overview

Before describing the modules in detail, a brief overview of all the hardware on a functional basis is given below:

The outstation is based on the 8085 microprocessor and operates on the SABUS system. It comprises the following hardware modules:-

(i) Central Processing Unit (SBC)

This is an 8085 single board computer (SBC) type SBC/2 (MK9) modified as described in paragraph 3.11.1. This is the only vendor supplied unit. This module provides the 4K of EPROM, 1K of RAM and the I/O port space required for the operating software; the 256 port I/O port space is divided into on-board (00H to 7FH) and off-board (80H to FFH) ports. Refer paragraph 3.12 for RAM, EPROM and I/O allocations.

(ii) Parameters, Watchdog and Timer module (PWT)

This module provides input parameters to the system, status indications, a periodic one second interrupt and a soft watchdog timer. This watchdog timer, as explained in paragraph 2.5.1(i), is the primary watchdog timer for the system.

(iii) Power indicator and watchdog timer module (PWR)

This module provides power supply indications and measuring points for the microprocessor power supply voltages. It also provides a hardware power-up reset and watchdog timer. This watchdog timer differs from the soft watchdog timer on the PWT module in that it will repeatedly reset the system until retriggered by the system software. This is the backup watchdog timer for the system. Refer paragraph 2.5.2(i) for more details.

(iv) Modem module (MODEM)

This demodulates incoming VFT messages from the u.h.f. radio receiver for the Serial Input Data (SID) line of the SBC module and modulates outgoing replies from the Serial Output Data (SOD) line of the SBC for the radio transmitter. It also automatically provides the necessary control signals for the radio (PTT), modulator (modulator on) and the SBC (clear-to-send) when initiated by a request-to-send from the SBC PA0 line. This has been discussed in paragraph 2.2.

(v) Analogue-to-digital converter module (A/D)

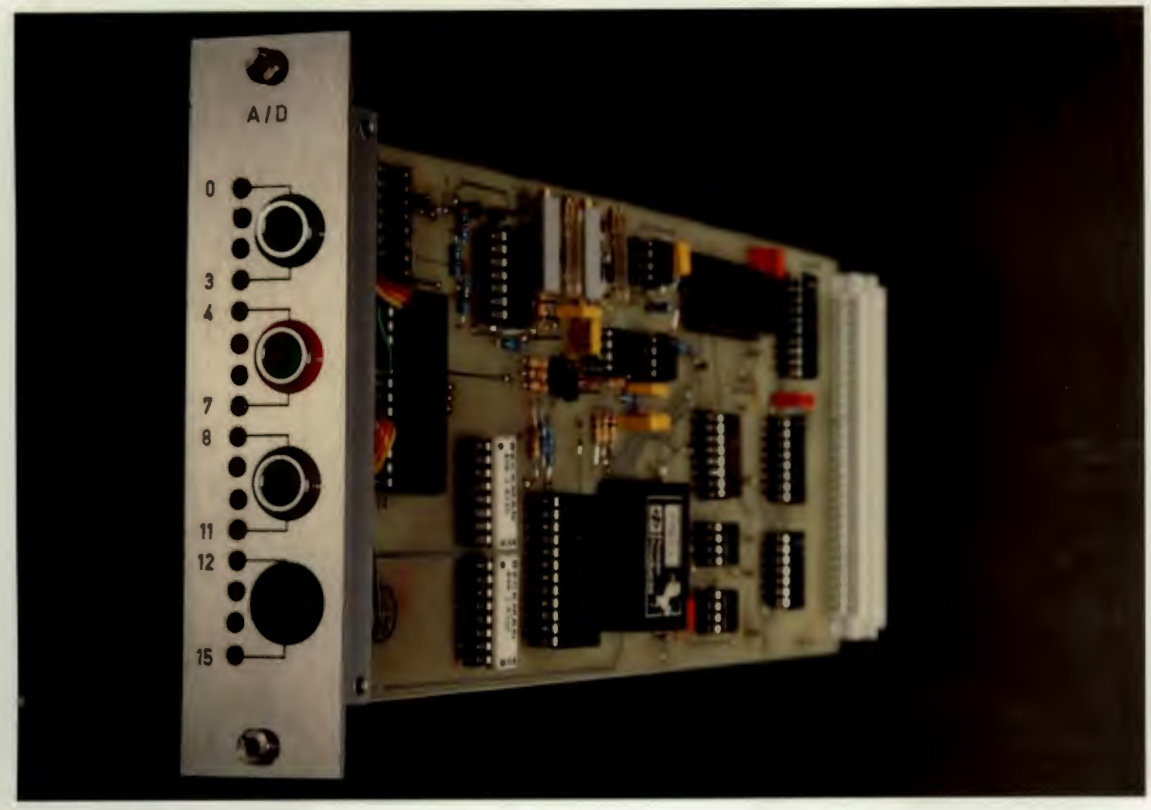
This provides eight or sixteen channels of opto-isolated analogue to digital conversion for level (where applicable) and flow rate measurands. This satisfies the requirements of paragraph 3.2

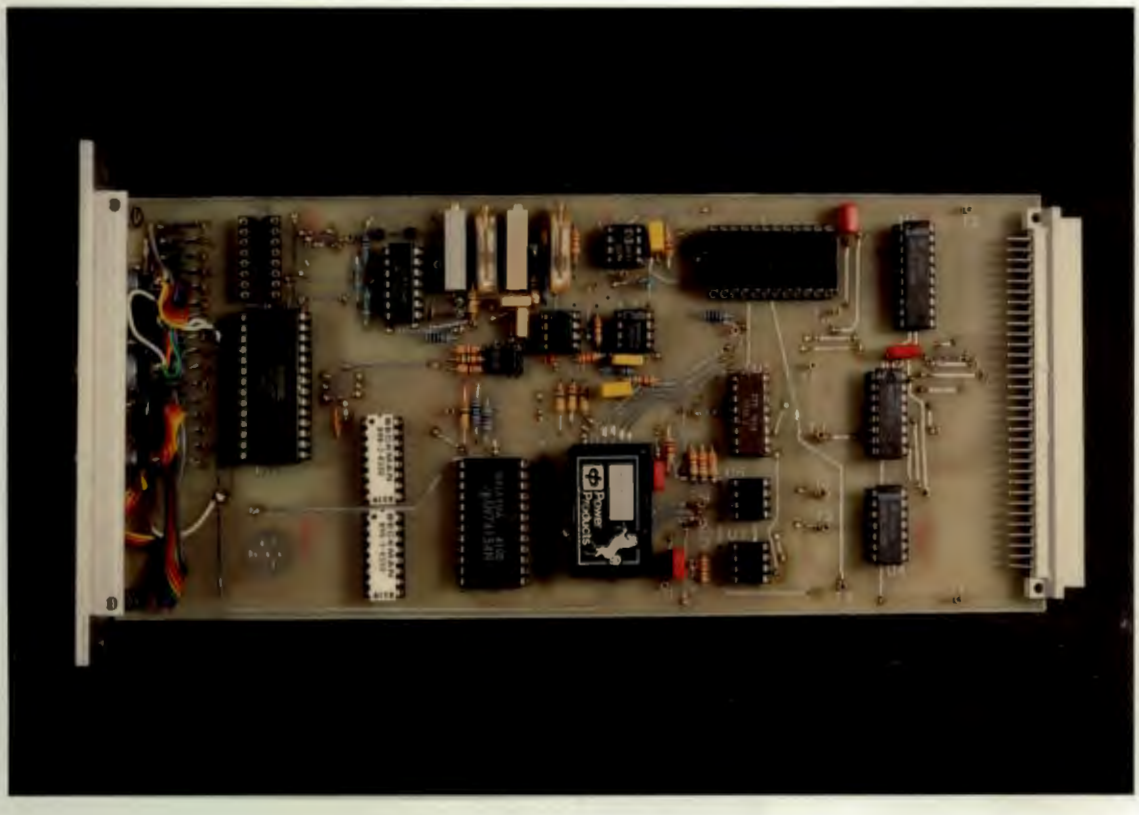
(vi) Digital input/output module (I/O)

This provides up to sixteen opto-isolated alarm inputs. This satisfies the requirements of paragraph 3.2.

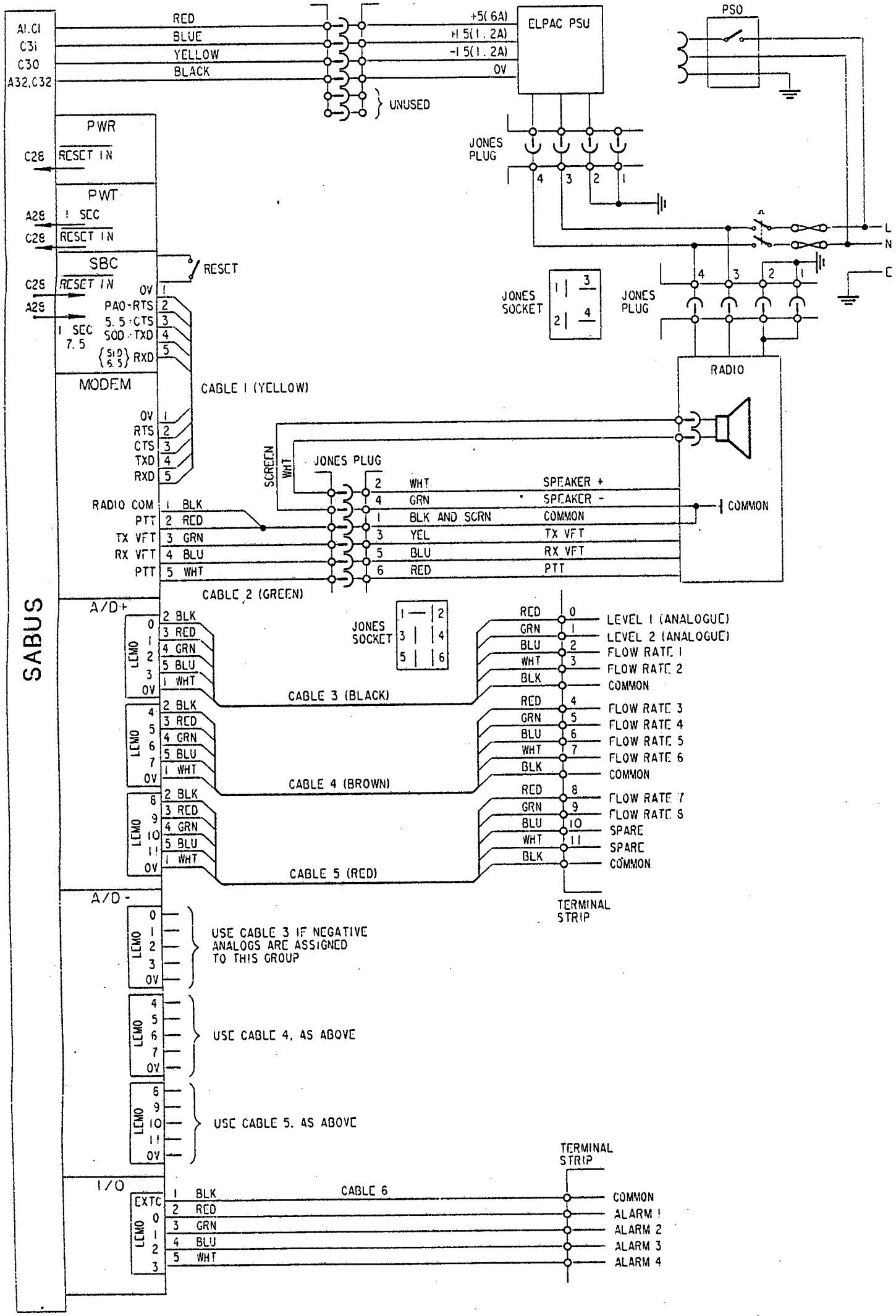
All these hardware modules are constructed in the same way with an aluminium front plate for mounting front panel components as appropriate. They are housed in a standard 19-inch card frame and plug into an S-64 backplane. Refer to photograph 3.1 for pictorial views of a typical hardware module.

For the interconnection of the modules described above, refer to Fig 3.1





PHOTOGRAPH 3.1 PICTORIAL VIEWS OF A/D MODULE



ELECTRICITY DEPARTMENT
CITY OF CAPE TOWN
CIVIC CENTRE

DRAWN: J.L
COMPILED: V.S ZAACKS
INFO.: J.DE V
CHECKED:

BLOCK DIAGRAM AND WIRING SCHEDULE | FIG 3.1

3.4 SABUS definition

Refer to Table 3.1 where the S-64 pin-assignments for the SABUS are given. Note that pins A28 and C28, which are not assigned on the standard SABUS, have been assigned to $\overline{\text{RST 7.5}}$ and $\overline{\text{RESET}}$ respectively. This was done to minimise external wiring between the SBC, PWT and PWR modules as shown in Fig 3.1. In all other respects, the outstation microprocessor bus is standard.

It should be noted that although the SABUS is ostensibly a standard bus and therefore should be processor independent, this ideal is not properly achievable in practice. It is in fact based on the INTEL philosophy; this is borne out by the presence of signals such as 'input read' and 'ouput write' which are typical of INTEL's port mapping of I/O space. ZILOG CPU's such as the Z80 can also be put on the SABUS since they use the same philosophy as INTEL.

The MOTOROLA 6800, on the other hand, does not lend itself readily to the SABUS. This is because the SABUS, like the 8085, is asynchronous whereas the 6800 uses a synchronous philosophy. During the early stages of the hardware development, a MOTOROLA 6840 PTM (Programmable Timer Module) was successfully interfaced to the SABUS but there were software restrictions eg if an 8085 HLT instruction occurs, the 8085 does not put out a clock signal onto the bus and so the MOTOROLA peripheral, which needs a synchronous clock, ceases to function! The writer is aware of other cases where the MOTOROLA 6800 CPU has been interfaced to the SABUS but again, with restrictions.

For this reason, all peripheral chips which were used on the outstation hardware modules are INTEL devices.

TABLE 3.1

SABUS DEFINITION

	C		A	
Supply	+5 V	1	+5 V	Supply
Data bus	DB 1	2	DB 0	Data bus
"	DB 3	3	DB 2	"
"	DB 5	4	DB 4	"
"	DB 7	5	DB 6	"
"	DB 9	6	DB 8	"
"	DB 11	7	DB 10	"
"	DB 13	8	DB 12	"
"	DB 15	9	DB 14	"
Address bus	AB 1	10	AB 0	Address bus
"	AB 3	11	AB 2	"
"	AB 5	12	AB 4	"
"	AB 7	13	AB 6	"
"	AB 9	14	AB 8	"
"	AB 11	15	AB 10	"
"	AB 13	16	AB 12	"
"	AB 15	17	AB 14	"
Non-maskable int	$\overline{\text{NMI}}$	18	CLK	System clock
Mem read	$\overline{\text{MR}}$	19	$\overline{\text{IR}}$	Input read
Mem write	$\overline{\text{MW}}$	20	$\overline{\text{OW}}$	Output write
Wait	$\overline{\text{WAIT}}$	21	$\overline{\text{RESET}}$	System reset
Hold (BUSRQ)	$\overline{\text{HOLD}}$	22	$\overline{\text{HOLDA}}$	Hold acknowledge
Interrupt request	$\overline{\text{INTR}}$	23	$\overline{\text{INTA}}$	Interrupt acknowledge
Mem latch (ALE)	$\overline{\text{SYNC}}$	24	$\overline{\text{M1}}$	Opcode fetch
Cascade int's	$\overline{\text{IN-INT}}$	25	$\overline{\text{OUT-INT}}$	Cascade int out
Bus available	$\overline{\text{BAVAIL}}$	26	$\overline{\text{REFRESH}}$	Bus avail refresh
Mem disable	$\overline{\text{MEMDIS}}$	27	NOT ASSIGNED	
	$\overline{\text{RESET}}$ *	28	$\overline{\text{RST 7.5}}$ *	
Bus request in	$\overline{\text{BUSRQ IN}}$	29	$\overline{\text{BUSRQ OUT}}$	Bus request out
	-12 V	30	NOT ASSIGNED	
	+12 V	31	NOT ASSIGNED	
	GND	32	GND	

* Bus modification - refer paragraph 3.4

3.5 Address decoding and data bus buffering

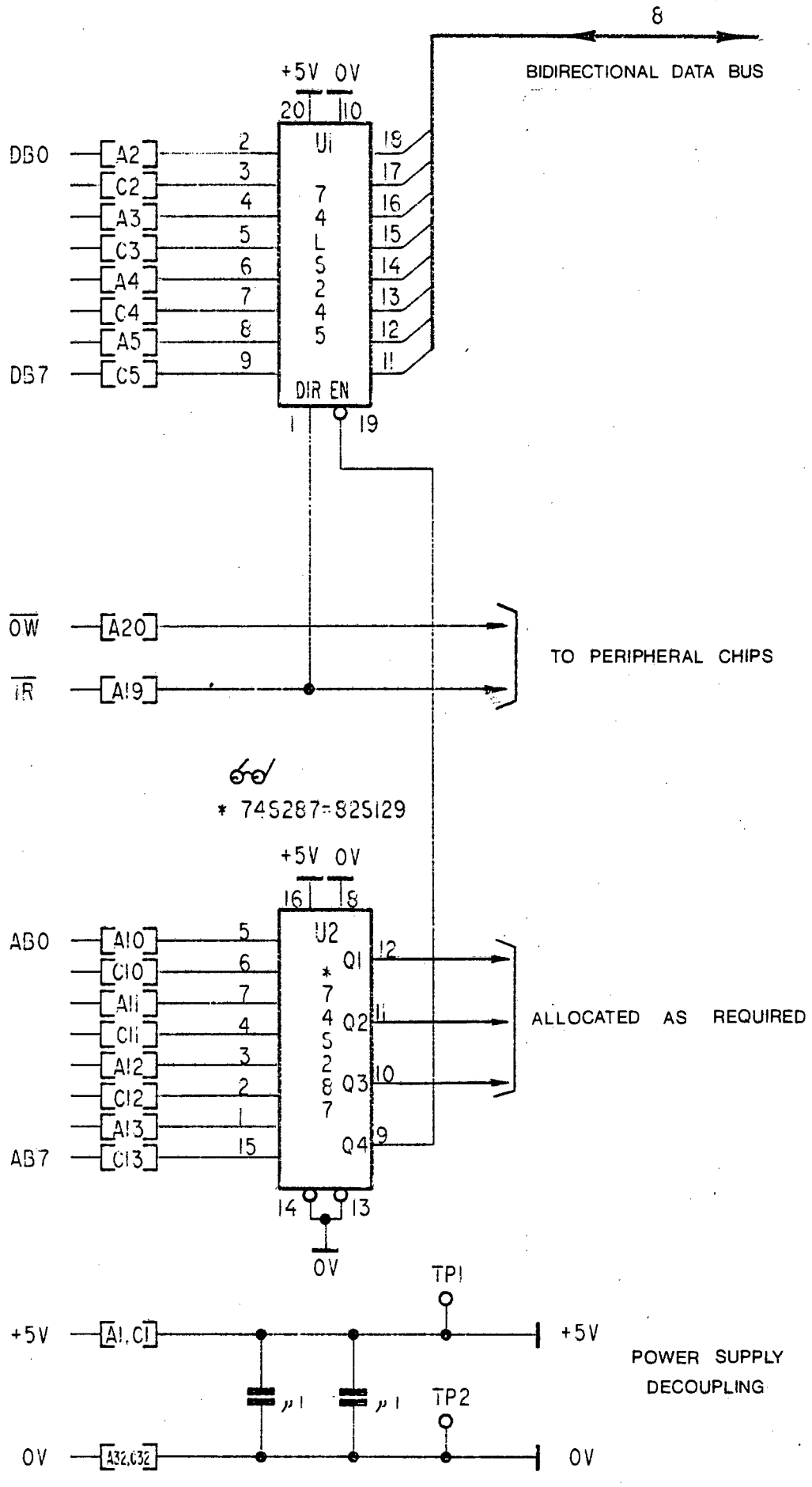
Before proceeding with the hardware modules individually, there is a section of the circuitry which is common to all the modules ie the address decoding and the data bus buffering, where applicable.

Refer to Fig 3.2. To reduce component count, the 74S287 (82S129) bipolar PROM was chosen as an address decoder. This 256 X 4 bit device also conveniently maps to the SABUS 256 I/O port address range. To use the device, select an address in the range 0 to FF hexadecimal and program the required bit pattern at that location, eg most peripheral chips have an active low chip select. This chip select is connected to, say, the Q2 data output of the PROM. At the same time that the peripheral chip is selected, the tri-state data bus buffer must be enabled. Its enable input could be connected to another data output of the PROM, say Q4. Therefore, in this case, the data pattern at this location will be 0101.

Note that many peripheral chips occupy more than one address location, four locations being typical in which case the base address and three consecutive locations in the PROM must contain the same bit pattern.

The data bus buffer's direction control is connected to the IR signal.

In the descriptions which follow, reference is made to modes of programming the INTEL 8254 Programmable Interval Timer. For further details, the reader should refer to the manufacturer's data sheet.



COMMON SABUS MODULE CIRCUITRY | FIG 3.2

3.6 Modem module (MODEM)

3.6.1 Theory of operation

Refer to Fig 3.3 for the complete circuit diagram.

3.6.1.1 Functions

(i) It provides the 1300Hz/1700Hz VFT signals as described in paragraph 1.5.1.

(ii) It satisfies the timing requirements of the telemetry communications described in paragraph 2.2.

(iii) It provides Tx and Rx VFT monitoring facilities as well as LED indications of the Tx and Rx status of the outstation.

3.6.1.2 Functional blocks

(i) Address decoding and data bus buffering

Refer paragraph 3.5

(ii) Modem and radio control

The three counters of U3 8254 are programmed as follows:-

Counter 0: Mode 1, hardware retriggerable one-shot with time-out counter loaded for 220 ms.

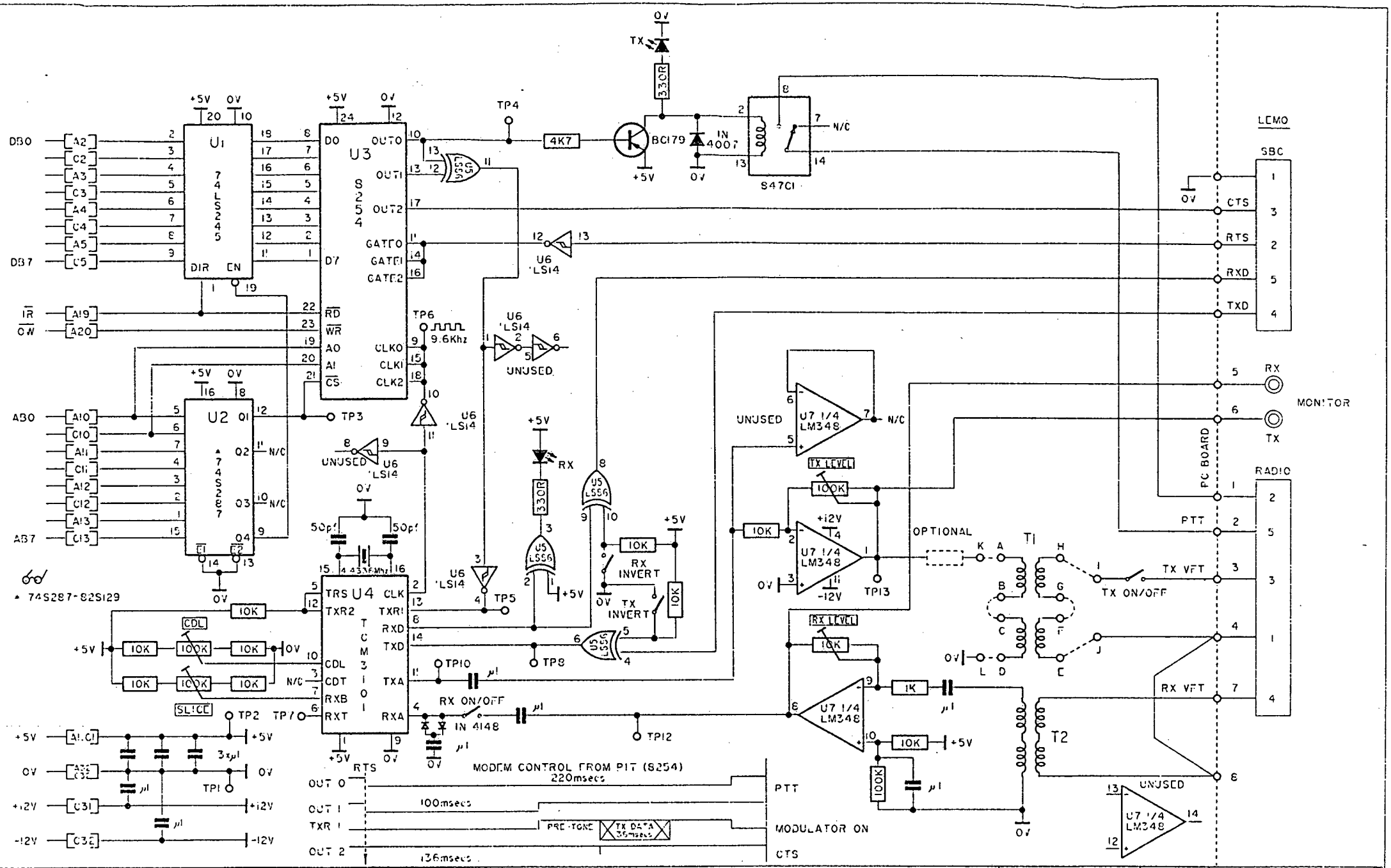
Counter 1: Mode 1, hardware retriggerable one-shot with time-out counter loaded for 100ms.

Counter 2: Mode 5, hardware triggered strobe with a strobe after 136 ms.

All three counters are triggered simultaneously by a RTS (request-to-send) signal from the SBC.

Out 0: This drives an isolation relay via the BC179 transistor to key the radio for 220ms.

Out 0 and Out 1: These two lines are exclusive OR'ed to switch the modulator of the TCM3101 modem chip on after 100ms. This allows for 100ms of radio warm-up time followed by 36ms of pretone after the RTS.



SABUS MODEM

CITY OF CAPE TOWN ELECTRICITY DEPARTMENT	DRAWN	J.DE V		SCALE	REV.
D/O MANAGER.	COMPILED	J.DE V			
	INFO.	J.DE V		FIG 3.3	
C.E.E. F.L.U.DANIEL	CHECKED				

Out 2: This sends a clear-to-send (CTS) 136ms after the RTS. This interrupts the 8085 CPU on the SBC on its RST 5.5 interrupt line; in this wa it signals to the CPU to send the Tx reply data stream.

Refer to the timing diagram on Fig 3.3. This satisfies the timing requirements of the telemetry communications discussed in paragraph 2.2.

(iii) Modem

The TCM 3101 (U4) is a self-contained modulator-demodulator using state of the art switched capacator technology for the filtering; it requires only the following external components for adjustments:-

(a) Trimpot and padder resistors for setting slicer level.

(b) Trimpot and padder resistors for setting carrier detect level. Carrier detect is not used for this project. Refer to Appendix N for the data sheet of this device.

(iv) Interface circuitry

Transformer T1 has four tappings. This provides the following ratios:-

3:1, 2:1, 1:1, 1:2, and 1:3 for Tx VFT line impedance matching. Refer paragraph 3.6.2 for configuration details.

Transformer T2 provides a 1:1 balanced line for Rx VFT.

Op-amps contained in U7 provide for Rx and Tx level adjustments via respective trimpots. These levels can be monitored at the monitor banana plugs on the front plates or at TP13 and TP12.

(v) Random logic

XOR gates in conjunction with switches provide for inversion of Rx and Tx digital data.

3.6.2 Modem module configuration and adjustments

3.6.2.1 Tx signal level

Adjust Tx level to the radio to 1V peak-to-peak with the TX LEVEL trimpot.

NOTE: A permanent Tx signal can be induced by lifting Pin 3 of U6. This is very useful when wanting to set up the deviation of the u.h.f. FM transmitter.

3.6.2.2 Rx signal level

Using the RX LEVEL trimpot adjust the Rx level at TP12 so that the Rx analogue signal to the TCM 3101 does not exceed 0.4 V peak-to-peak.

3.6.2.3 Slicer level

Connect an oscilloscope to TP9 to monitor the Rx digital data stream. Adjust the slicer level using the SLICE trimpot for a bit time of +/- 1.66 ms. If the card is plugged into a running outstation with a valid address the 'RX VAL' LED of the PWT module will come on followed by the 'TX' LED of both the MODEM and PWT modules if this adjustment is correct.

3.6.2.4 Switch selections

(i) RX must be inverted, TX not inverted. The reason for these polarities can be appreciated when Fig 1.3 and 4.4 are referred to:-

In the absence of any VFT signal, the demodulator output is low; when the 1300Hz pretone of the request word begins, it goes high; this must cause the Rx routine to be entered by generating an RST 6.5 interrupt. The 8085 RST 6.5 interrupt signal is a high logic level; therefore the demodulator output has the required polarity. Since an inverter precedes the RST 6.5 input line of the CPU on the SBC module (refer to Fig 3.8), another inversion is required; this is provided by the MODEM module.

For the reply word, the pretone must be 1700Hz ie a low logic level to the modulator input; this implies a high logic level for the start bit (so that it can be detected as such by the master station); since the Rx routine sets the start bit to a high logic level, it has the correct polarity; however, the SOD line of the CPU is followed by an inverter on the SBC module (refer Fig 3.8) and so another inversion has to be done. This is done by the Rx routine, so data inversion by the MODEM module is not required.

(ii) Insure that RX and TX are on.

3.6.2.5 Tx transformer wire-wrap options

There are four windings on transformer T1: AB, CD, EF and GH. This allows for five ratios ie 3:1, 2:1, 1:1, 1:2, 1:3.

For this project use 1:1 ie wire-wrap K-A, B-C, D-L, E-J, F-G and H-I.

3.6.2.6 Tx transformer impedance matching

An optional resistor can be inserted between Pin 1 of U7 and wire-wrap Pin K for impedance matching. This is often required when the modem transmitter is connected to a telephone line in parallel with other outstations; the output impedance of each outstation loads the line and hence the higher the output impedance the less the loading ie a current-source rather than a voltage-source is desirable. Remember that the optional resistor has an effective value of the SQUARE of the turns ratio of the Tx matching transformer

Example: If a 1K resistor is fitted and the 1:3 ratio selected, this appears as 9K at the secondary of the transformer; this is usually high enough for telephone work.

3.6.2.7 Mapping PROM

The contents of the PROM are listed below:-

00	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
10	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
20	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
30	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
40	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
50	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
60	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
70	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
90	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	06	06	06	06
C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the mapping PROM contents.

3.7 Parameters, Watchdog and Timer module (PWT)

3.7.1 Theory of operation

Refer to Fig 3.4 for the complete circuit diagram.

3.7.1.1 Functions

(i) Input parameters are supplied to the system via thirty-two dual-in-line switches. These can be allocated according to the requirements of the system.

(ii) Eight status indicator LED's are provided to give indications system operation as an aid to fault finding. These are soft and can also be allocated according to system requirements.

(iii) The programmable RST 7.5 interrupt can be used to interrupt the system as required. RST 7.5 was chosen as it is a latched interrupt and can therefore be interrogated retrospectively should a higher level routine be operative when the interrupt occurs.

(iv) A soft watchdog timer which has a programmable time-out period and must be continuously retriggered by an output-write instruction at the appropriate port address in the system software otherwise it will restart the system.

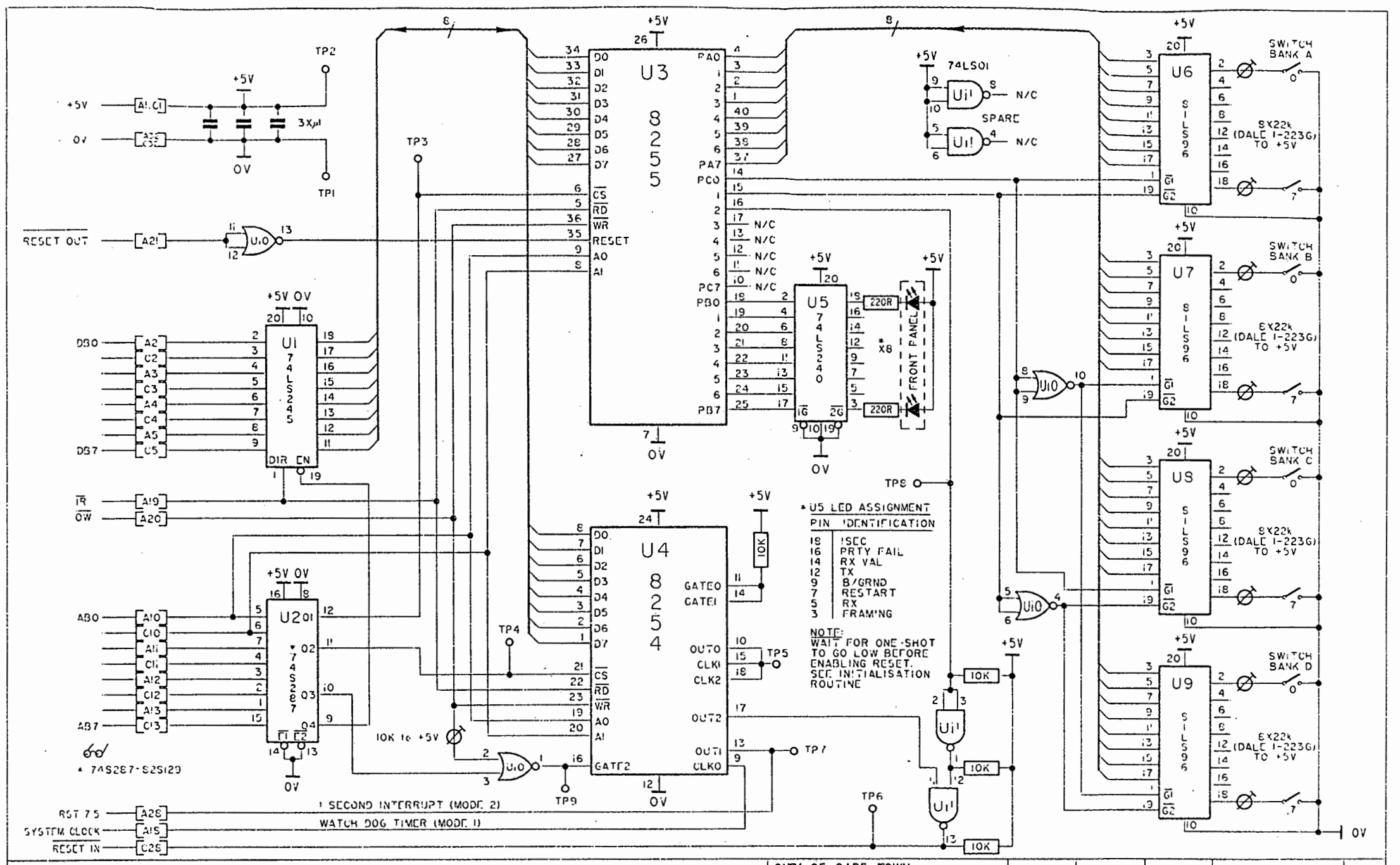
3.7.1.2 Functional blocks

(i) Address decoding and data bus bufferring

Refer paragraph 3.5.

(ii) Parameter input

This comprises Port A and PC0 and PC1 of Port C of the 8255 (U3), four 81LS96 (U6-U9) tri-state octal buffers and thirty-two dual-in-line input switches arranged as four 8-bit banks, A to D.



SABUS PWT MODULE

CITY OF CAPE TOWN ELECTRICITY DEPARTMENT	DRAWN	J.LUSTY		SCALE	REV.
	COMPILED	C S			
D/O MANAGER.	INFO.	J.DE V			
C.E.E. F.L.U.DANIEL	CHECKED				

FIG 3.4

Port A is programmed for input only, port C as an output. Outputting binary 0-3 on bits PC0 and PC1 selects one of the four octal buffers U6-U9 enabling the status of the respective bank of eight dual-in-line switches to be read at port A.

(iii) Status indicator LED's

Port B is programmed for output and drives the LED's via U5 (74LS240); these LED's can be wired as required.

(iv) 8254 Programmable interval timer

Counter 0: This is programmed for rate generation (mode 2). This is used to prescale the 3.072 MHz system clock so its output can feed counters 1 and 2 with a usable lower frequency.

Counter 1: This is also programmed for rate generation (mode 2) eg in this project this counter is loaded to generate a 1 Second interrupt.

Counter 2: This is programmed as a hardware retriggerrable one-shot to provide a watchdog timer. This counter is loaded for a time-out period of +/- 1.5 s; thus if the gate input of Counter 2 is not retriggered within this time by the outstation software the counter will time out and reset the system. This is the soft watchdog timer as discussed in paragraph 2.5.1 (i). If PC2 is high, this reset facility is disabled.

3.7.2 PWT module configuration

3.7.2.1 Switch banks

There are four banks of eight dual-in-line switches used to parameterise each outstation. These are set as follows:-

Bank A

Switch 1 - 5	Outstation address; switch 1 = LSB.
Switch 6	Unused
Switch 7	ON = mixed polarities on analogue channels. See note below.
Switch 8	ON = digital levels; OFF = analogue levels. Refer paragraph 3.2

NOTE: If analogues of different polarities are required, positive analogues are connected to the first A/D module and the negatives to the second A/D module. Thus the channels are mutually exclusive; so if channel 0 is positive no negative analogue can be connected to the corresponding channel on the second A/D module and must be assigned to a channel not used by a positive analogue input. The software implications of this are discussed in Appendix J.

Note that only ten channels are catered for in this system as required in paragraph 3.2.

Bank B

This selects analogue flow rates from analogue channels 2 through 9 (analogue channels 0 and 1 are used for levels where applicable) for integrated flow rate 1.

NOTE: Analogue channels 2 - 9 correspond with flow rates 1 - 8 which correspond with switches 1 - 8.

Refer to Appendix F.

Bank C

This is as above but for integrated flow rate 2.

Bank D

This is as above but for integrated flow rate 3.

3.7.2.2 Status indicator LED's

Refer to Fig 3.4 where the assignment of the LED's is given.

3.7.2.3 Mapping PROM

The contents of the PROM are listed below:-

00	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
10	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
20	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
30	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
40	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
50	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
60	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
70	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
90	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
E0	06	06	06	06	05	05	05	05	0B	0F	0F	0F	0F	0F	0F	0F
F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the mapping PROM contents. Note that this module and the PWR module have their one-shots mapped to the same port address so that they may be simultaneously triggered by the software as explained in paragraph 2.5.2 (i); refer paragraph 3.10.2.

3.8 Analogue-to-digital converter module (A/D)

3.8.1 Theory of operation

Refer to Fig 3.5 for the complete circuit diagram.

3.8.1.1 Function

This module provides sixteen or eight analogue input channels, isolated from the microprocessor supply.

NOTE: For sixteen input channels positive or negative signals can be connected but they must all be of the same polarity. For eight channels only positive signals may be used.

3.8.1.2 Functional blocks

(i) Address decoding and data bus buffering

Refer paragraph 3.5.

(ii) Channel selection and display

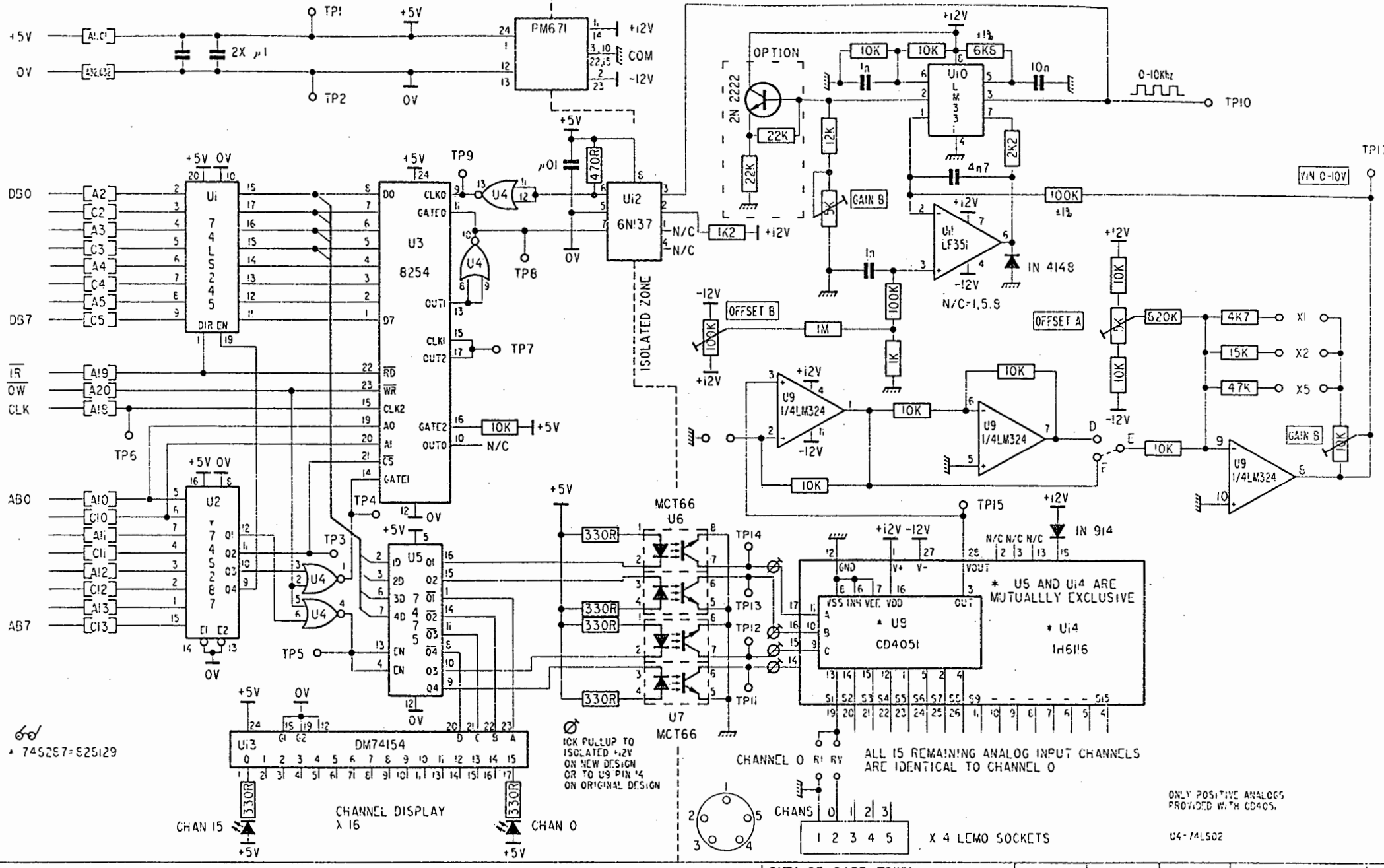
When an output-write is executed to the port address selected in the address decoding PROM (U2), channel data will be strobed into the quad latch U5. Its Q outputs drive U6 and U7 opto-couplers to select the required channel of the multiplexer (U8 or U14). The Q outputs drive a 4-16 line decoder (U13) which in turn drives the selected channel LED.

(iii) Frequency counter and voltage-to-frequency converter [1]

The PIT (U3) counts the opto-coupler pulses from the voltage-to-frequency converter (V/F).

This function is achieved as follows:-

Counter 0 is programmed for interrupt on terminal count (Mode 0). Thus before a conversion is initiated this counter is loaded with FFFF hexadecimal. The counter will be decremente by 1 for each pulse received from the V/F while its gate input is high.



S.A.BUS 16/8 CHANNEL GALVANICALLY ISOLATED A/D CONVERTER

CITY OF CAPE TOWN ELECTRICITY DEPARTMENT	DRAWN	J.L		SCALE	REV.
D/O MANAGER.	COMPILED	R.W			
	INFO.	J.DE.V		FIG 3.5	
C.E.E. D.C.PALSER	CHECKED				

Counter 1 is programmed as a hardware retriggerable one-shot (Mode 1). The counter is loaded to produce a one-shot time of one second. The one second window at OUT 1 is used to control the gate input of Counter 0 enabling counting of pulses from the V/F.

Counter 2 is programmed as a rate generator (Mode 2). This prescales the 3.072 MHz system clock to a lower frequency to drive the clock input of Counter 1.

The conversion sequence is as follows:-

(i) Load Counter 0 with FFFF hexadecimal.

(ii) Start the conversion by an output-write to port assigned to trigger the gate input of Counter 1.

(iii) Wait for at least one second then read the contents of Counter 0 and complement the 16-bit value. This gives the frequency from the V/F in Hz which is directly proportional to the input voltage at the V/F ie

0 to 10 kHz corresponds with 0 to -10 V.

(iv) Analogue input signal conditioning is provided by three op-amps in U9. Refer paragraph 3.8.2.

(v) Analogue channel multiplexing:

This is provided by U8 or U14; note that these IC's are mutually exclusive. Refer paragraph 3.8.2.

(vi) Isolated +12 V and -12 V is provided by a type PM671 DC/DC converter. This provides an isolated supply for the analogue circuits of this module.

Refer to Appendix N for data sheets of the analogue multiplexer (U14), the high speed optocoupler (U12) and the DC/DC converter module.

3.8.2 A/D module configuration and adjustments

3.8.2.1 Channel input options

(i) Eight or sixteen analogue inputs:

(a) If only eight analogue inputs are required insert a 4051 in U8, leave U14 empty. Note that only positive analogues can be accomodated. Refer to Fig 3.5

(b) For sixteen analogue inputs use an Intersil 6116 or equivalent in U14; U8 must then be empty.

(ii) Current or voltage inputs:

(a) Current inputs:

Select RI to produce an input voltage at the analogue multiplexer (U8 or U14) not in excess of 10 V for maximum current.

eg: For a 4-20 mA transducer use a 500 ohm resistor 2-10 V.

(b) Voltage inputs:

Select RV and RI to form a voltage divider to keep the maximum input voltage at a magnitude of 10 V.

3.8.2.2 Input signal conditioning

(i) For positive input signals wire-wrap pins F and E.

(ii) For negative input signals wire-wrap pins D and E.

(iii) Select wire-wrap multiplier option (X1, X2 or X5) to obtain -10 V at the input of the voltage-to-frequency converter for maximum input signal.

NOTE: An additional X2 can be obtained by fitting a 10K resisto between point C and ground.

3.8.2.3 Mapping PROM

The contents of the PROM are listed below:-

00	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
10	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
20	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
30	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
40	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
50	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
60	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
70	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80	05	05	05	05	0B	06	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
90	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the mapping PROM contents.

3.8.2.4 Adjustments

(i) Input voltage to the voltage-to-frequency converter (TP17)

(a) Set GAIN A (GA) to maximum ie fully clockwise.

(b) Ground the selected input channel (this defaults to 15 or 7 on power-up).

(c) Adjust OFFSET A (OA) to give 0 V at TP17. Use the millivolt range of the voltmeter for maximum accuracy.

(d) Connect a variable voltage or current source to the selected input channel, depending on input channel configuration. Connect voltmeters to TP15 and TP17. Adjust GAIN A (GA) so that the voltage at TP17 tracks the input voltage at TP15 multiplied by the gain factor selected.

NB: Input voltage to the voltage-to-frequency converter at TP17 must not exceed -10 V.

(ii) Offset and gain of voltage-to-frequency converter

(a) Ground the selected input channel.

(b) Adjust OFFSET B (OB) to just above 0 Hz at TP10.

(c) Connect a variable voltage or current source to the selecte input channel depending on input channel configuration.

(d) Adjust GAIN B (GB) so that the output frequency at TP10 tracks the input voltage at TP17 as follows:-

0 to 10 kHz for a 0 to -10 V range.

The A/D boards used in this project are configured as follows:-

(i) Intersil 6116 or equivalent in U14; U8 empty. This satisfies the analogue input requirements discussed in paragraph 3.2

(ii) The following table covers most input signals likely for the outstations:-

INPUT	WIRE-WRAP LINKS	WIRE-WRAP MULTIPLIER	INPUT RESISTOR
0 to 5 mA	E - F	X 2	1K
0 to 10 mA	E - F	X 1	1K
0 to 20 mA	E - F	X 1	500R *
4 to 20 mA	E - F	X 1	500R *

* If this value is not available, a 470R resistor may be used in which case the GAIN A (GA) control, when adjusted as in paragraph 3.8.2.4(i)(d) above, can be used to compensate for the slightly different resistor value.

NOTE: It is preferable to use a metal film or metal oxide 2 % tolerance resistor and NOT a 5% carbon film or carbon composition resistor for the input resistor.

3.9 Digital input/output module (I/O)

3.9.1 Theory of operation

Refer to Fig 3.6 for the complete circuit diagram.

3.9.1.1 Function

This module provides eight relay isolated outputs with feedback and eight opto-isolated inputs. However, further inputs may be obtained by using the feedback section of an unused output channel. Any external system voltage, polarity and switching arrangement can be accomodated for each group of eight input or output channels. Refer paragraph 3.9.2 for further details.

3.9.1.2 Functional blocks

(i) Address decoding and data bus buffering

Refer paragraph 3.5.

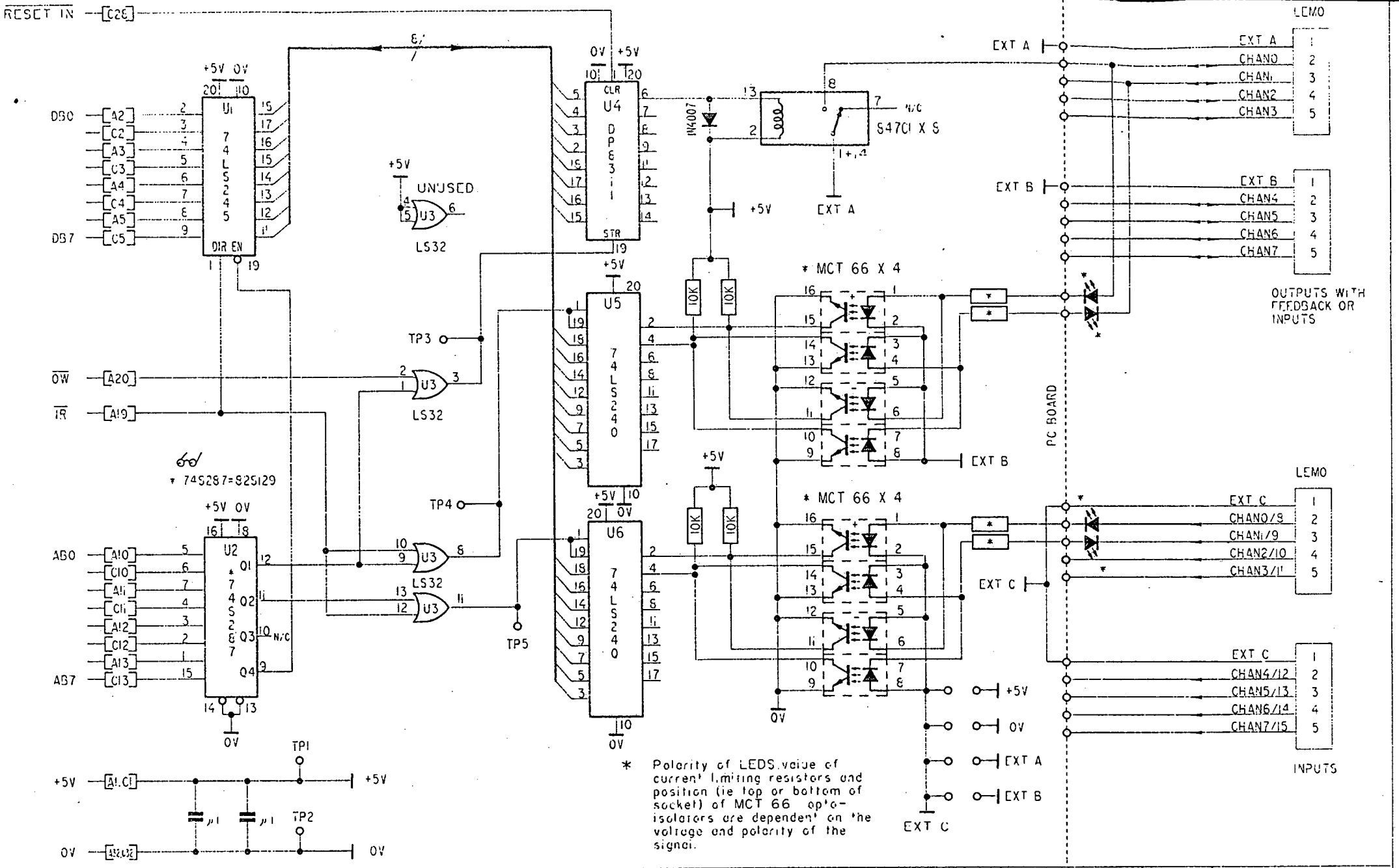
(ii) Output and feedback section

This comprises a DP8311 latch (U4) and up to eight type 847C1 mercury-wetted relays. Each relay switches EXT A to the output circuit and a type MCT66 opto-coupler via a channel selection LED for indication. The output of the opto-coupler drives the feedback input buffer 74LS240 (U5). The output latch and this input buffer are mapped at the same port address, so to use the feedback feature, write the required output data to the latch, allow for relay settling time, and then read back the feedback data from the input buffer.

(iii) Input section

The input section is identical to the feedback section describe above. This allows unused outputs to be assigned as additional inputs. The data is read from input buffer U6 and is mapped one address higher than the output port.

Refer to Appendix N for the data sheet of the DP8311 latch.



S.A.BUS I/O MODULE

CITY OF CAPE TOWN ELECTRICITY DEPARTMENT	DRAWN	J.L		SCALE:	REV
D/O MANAGER.	COMPILED	R.W			
	INFO.	J.DE V		FIG 3.6	
C.E.E. D.C.PALSER	CHECKED				

3.9.2 I/O module configuration

3.9.2.1 Output/input port

(i) Connect the switched potential to EXT A.

(ii) Connect the return of the external system to EXT B if feedback required.

(iii) If EXT A is positive with respect to EXT B then install the MCT66 opto-isolator in the upper half of the appropriate socke as indicated on the circuit board. If EXT A is negative with respect to EXT B then the MCT66 must be installed in the lower half of the appropriate socket. In each case the indicating LED, if required, must be polarised accordingly; otherwise replace it with a strap if feedback still required.

(iv) Select current limiting resistors to give between 10 and 20 mA in the feedback opto-isolator circuits. Ensure that resistors are of sufficient wattage!

Unused output channels can have their relays omitted and the corresponding input pins on the LEMO connectors can be used as additional inputs if the EXT A/B potential assignment is suitable.

3.9.2.2 Input section

(i) The return of the input signal is connected to EXT C via pins 1 of the input LEMO connectors. However, if required, EXT C may be connected to either internal system 0v or +5v, or EXT A or EXT B via a patch bay.

(ii) If EXT C is negative with respect to the input signal, install the MCT66 opto-isolator in the upper half of the appropriate socket as indicated on the circuit board.

If EXT C is positive with respect to the input signal, install the MCT66 opto-isolator in the lower half of the appropriate socket. In each case the indicating LED, if required, must be polarised accordingly; otherwise replace it with a strap.

(iii) Select current limiting resistors to give between 10 and 20 mA in the opto-isolator circuits. Ensure that resistors are of sufficient wattage!

The exact configuration of the EXT A, EXT B and EXT C connections may vary from site to site and should be determined by inspection.

3.9.2.3 Mapping PROM

The contents of the PROM are listed below:-

00	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
10	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
20	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
30	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
40	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
50	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
60	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
70	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
80	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
90	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
A0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
B0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
C0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
D0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F
E0	0F	0F	0F	0F	0F	0F	0F	0F	0F	06	05	0F	0F	0F	0F	0F
F0	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F	0F

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the mapping PROM contents.

3.10 Power indicator and watchdog timer module (PWR)

3.10.1 Theory of operation

3.10.1.1 Functions

This module has two independent functions:-

(i) It indicates the presence of +5 V and - 12 V on the SABUS power rails as mentioned in paragraph 2.5.2(ii).

(ii) It restarts the software programme via the $\overline{\text{RESET IN}}$ line on the SABUS if the software stops running ie it provides a watchdog timer function. This was discussed in paragraph 2.5.2(i).

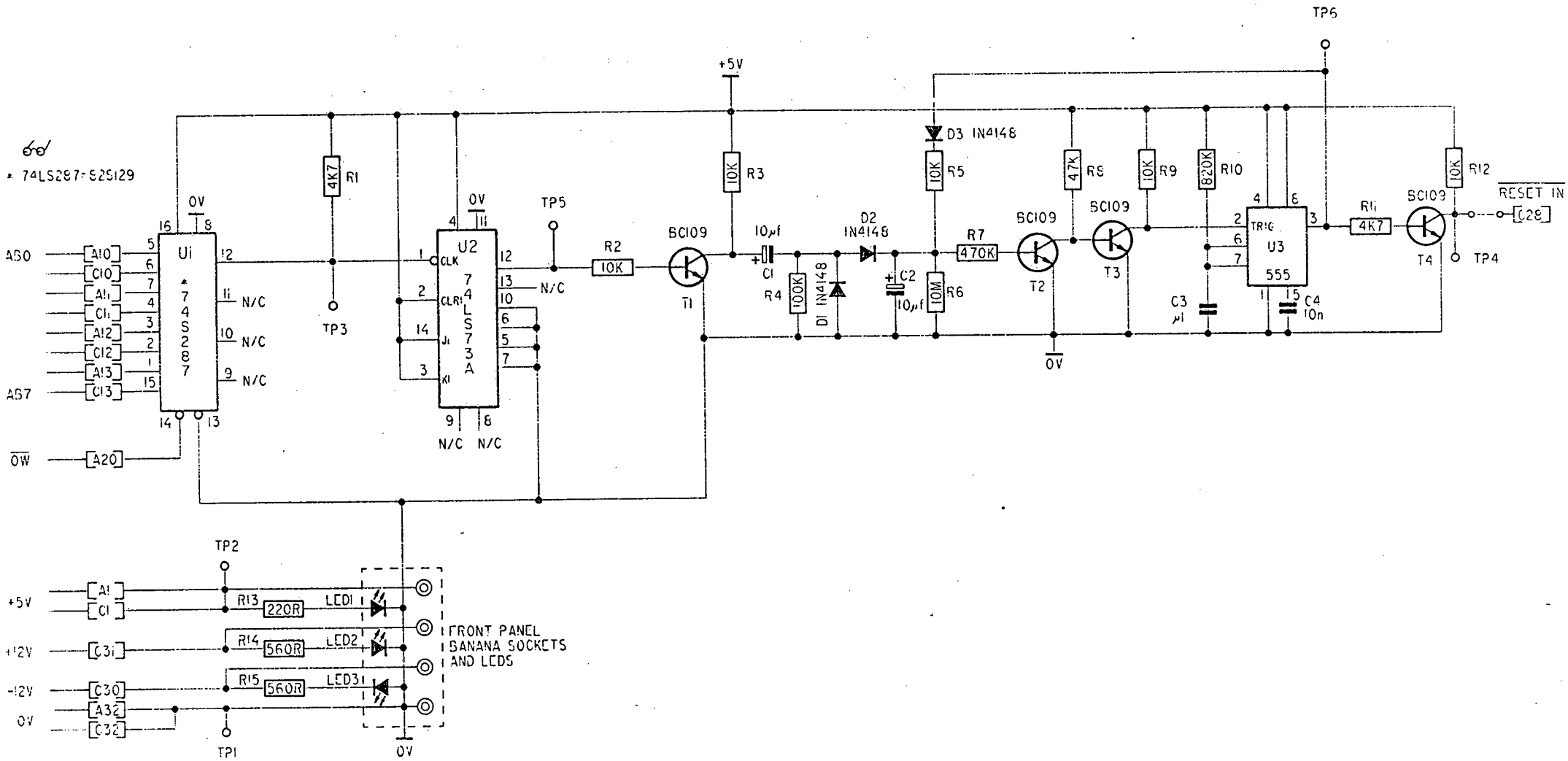
3.10.1.2 Operation

Refer to the circuit diagram Fig 3.7 for the detailed explanation which follows:- [2]

R13, R14, R15, LED1, LED2 and LED3 perform the power rail monitoring and the circuit is self explanatory. The LED's are front panel mounted together with four banana sockets ie three for the three SABUS power rail voltages and one for the 0 V common.

The watchdog timer is essentially a free running multivibrator with an inhibit input which becomes active when it is toggled above a certain minimum rate. It operates as follows:-

U1 is a Schottky TTL PROM which is programmed to decode an output-write instruction at a particular port address. This produces a very narrow negative spike (microseconds) at TP3; R1 ia a pull-up resistor. This narrow spike is used to clock U2, a J-K flip-flop, to produce a square-wave at TP5. R2, R3 and T1 buffer this signal and this is used to keep C2 positively charged via C1, R4, D1 and D2. R7, R8, R9, T2 and T3 form a non-inverting buffer so T3's collector is high and U3 one-shot pin 3 is low. This condition will persist for as long as the software toggles U2 frequently enough; if this is not the case, C2 will eventually discharge into R6 until its voltage falls below the threshold of T2; this causes a positive transition at the collector of T2 which becomes a negative transition



S.A.BUS POWER INDICATION AND WATCHDOG TIMER

CITY OF CAPE TOWN ELECTRICITY DEPARTMENT	DRAWN	J L		SCALE	REV.
D/O MANAGER.	COMPILED	R W			
	INFO	J DE V		FIG 3.7	
C.E.E. D.C.PALSER	CHECKED				

at the collector of T3 which triggers U3 one-shot. U3 Pin 3 goes high which discharges C2 via D3 and R5. Eventually, C2 charges up to the point that T3's collector goes high again; also, when the one-shot time period has expired, U3 Pin 3 goes low and C2 starts to discharge into R6 again; this cycle is repeated, thus forming an astable multivibrator for as long as U2 is not toggled by the software. R11, R12 and T4 form an inverting buffer. Thus, reset pulses from T4's collector will continue to be applied to the $\overline{\text{RESET IN}}$ line of the SABUS for as long as the software does not start to run.

Note that for proper operation of this circuit the one-shot timer as determined by R10 and C3 must be of sufficient duration to charge C2 up to the point where T2 turns on to reset the trigger pulse at U3 Pin 2; this is determined mainly by R5 and C2. With the values shown, a reset pulse of 90 ms occurs every fifteen seconds in the absence of a software generated toggle signal at TP5 as mentioned in paragraph 2.5.2 (i).

3.10.2 PWR module configuration

The only configuration required is the programming of the mapping PROM, the contents of which are listed below:-

```
00 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
10 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
20 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
30 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
40 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
50 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
60 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
70 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
80 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
90 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
A0 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
B0 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
C0 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
D0 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
E0 0F 0F 0F 0F 0F 0F 0F 0F [0E] 0F 0F 0F 0F 0F 0F 0F
F0 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F 0F
```

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the mapping PROM contents.

Note that this module and the PWT module have their one-shots mapped to the same port address so that they may be simultaneously triggered by the software, the PWR module's hard watchdog being the backup for the PWT module's soft watchdog described in paragraph 3.7.1.1(iv). This watchdog backup concept was discussed in paragraph 2.5.2(i).

3.11 Central Pocessing Unit (SBC)

This is the only purchased hardware module in the system. Refer to Fig 3.8 for the complete circuit diagram. It has been slightly modified to suite the requirements of this project; these modifications are indicated by exclamation marks (!) or arrows on Fig 3.8.

3.11.1 SBC modifications

3.11.1.1 Increased I/O map

With the standard SBC 8085 board, external I/O is limited to the address range C0 - FF hexadecimal. The external I/O range was expanded to 80 - FF hexadecimal by using address line AD7 instead of AD6 as the linear select line for the on-board 8255A. This forfeits the availability of the 8251 USART which must be removed from its socket IC8.

The mapping PROM (74S287 or 82S129) contents also had to be modified to select the bus buffers for the increased I/O.

3.11.1.2 New mapping PROM contents

```
00 07 0D 07 0E 0F 0F 0F 0F 0B 0E 0B 0E 0F 0F 0F 0F
10 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
20 07 0E 07 0E 0F 0F 0F 0F 0B 0E 0B 0E 0F 0F 0F 0F
30 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
40 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
50 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
60 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
70 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
80 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
90 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
A0 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
B0 0E 0E 0E 0E 0F 0F 0F 0F 0E 0E 0E 0E 0F 0F 0F 0F
C0 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
D0 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
E0 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
F0 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E 0E
```

Refer paragraph 3.5 and the MAP module of the software in paragraph 3.12 for an explanation of the new mapping PROM contents.

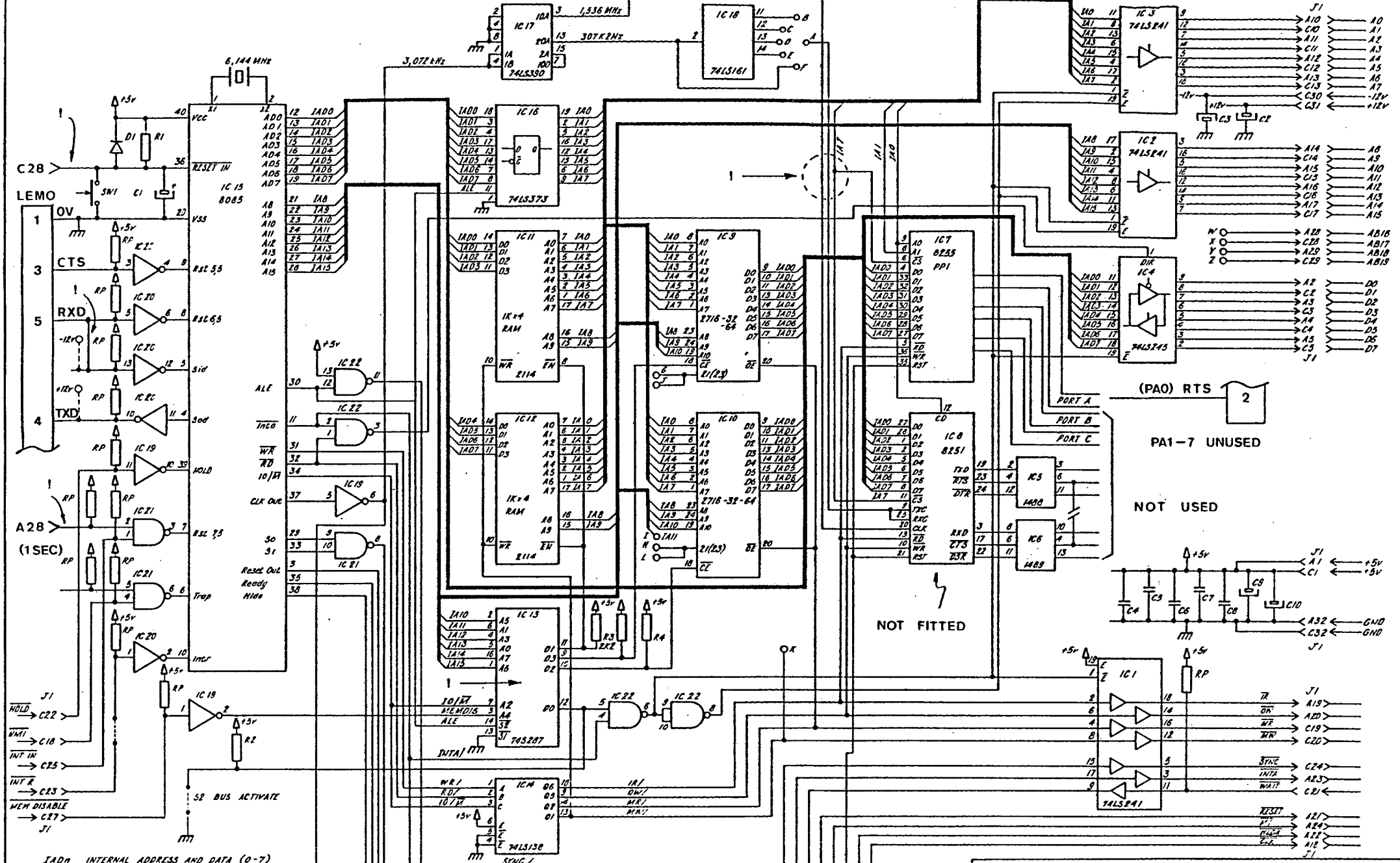


FIG 3.8

BASIC ELECTRONICS

8085 SBC2 (MODIFIED VERSION 1)

DESIGNED	J. MORROW	DRAWN	L. BUCHLY	APPROVED
DATE	6-5-86	SHEET 1 OF 1		Nº 502 REV 9

3.11.1.3 Reset

The oustation soft and hard watchdog timers discussed in paragraph 2.5 require a bus line to reset the CPU. As the standard SABUS does not provide for this, a spare bus line C28 was assigned for use as a RESET IN to the CPU. Thus the SBC must be modified by connecting a wire between C28 and the $\overline{\text{RESET IN}}$ Pin 36 of the SBC.

3.11.1.4 1 Second interrupt

As it was desirable to have the 1 Second interrupt from the PWT on the SABUS, spare bus line A28 was allocated to this. Thus modify the SBC by connecting a wire between A28 and Pin 7 of the resistor pack (IC R/P). This connects A28 to the RST 7.5 interrupt.

3.11.1.5 Modem control signals

The standard 37-way D connector must be removed as only five modem control signals are required at the front plate of the SBC. These signals are connected to a 5-way LEMO socket as follows:-

LEMO	SIGNAL	D CONNECTOR
1	N/C	
2	RTS - PORT A BIT 0	29
3	CTS - RST 5.5	20
4	TXD - SOD	22
5	RXD - (SID ((RST 6.6	3)) * 2)
		* See NOTE 2

NOTE 1: The LEMO socket is numbered anti-clockwise facing the front panel.

NOTE 2: A link between solder pads 2 and 3 of the removed 37-way D connector is installed.

3.11.2 SBC configuration

The SBC is configured for 2 X 2732 EPROM's in IC9 and IC10 ie 8K of EPROM from 0 to 1FFF hexadecimal for the software. There is 1K of RAM from 2000 to 23FF hexadecimal.

3.12 Hardware mapping

A listing of the MAP module of the software is included here for completeness because it contains all the mappings of the SABUS hardware modules discussed above.

ISIS-II 8080/8085 MACRO ASSEMBLER, V4.0 MAP PAGE 1

```
LOC  OBJ        LINE        SOURCE STATEMENT

                  1 $OBJECT(:F1:MAP.LNK) MOD85 DEBUG XREF MACROFILE
                  2         NAME    MAP
                  3         PUBLIC  CHNUM
                  4         PUBLIC  TPRAM,BTRAM
                  5         PUBLIC  MODEM,MCNTRL,LSALM,BCD124,OPTO1
                  6         PUBLIC  BCD101,BCD123,OPTO2,BCD201,BCD223,OPTO3
                  7         PUBLIC  MSALM,OPTO4
                  8         PUBLIC  PARM,STATUS,PRTSEL,PWT
                  9         PUBLIC  ACTR0P,ACTR1P,ACTR2P,ACNWDP,ONESHT
                 10         PUBLIC  ACTR0N,ACTR1N,ACTR2N,ACNWDN
                 11         PUBLIC  CHNSEL,STRCNV
                 12         PUBLIC  MCNTR0,MCNTR1,MCNTR2,MCNTWD
                 13         PUBLIC  PCNTR0,PCNTR1,PCNTR2,PCNTWD
                 14 ;
                 15 ;
000A             16 CHNUM    EQU     10D             ;NUMBER OF ANALOGUE CHANNELS
                 17 ;
                 18 ;
                 19 ;****************************** RAM LIMITS ************************************
                 20 ;
2000             21 BTRAM    EQU     2000H           ;BOTTOM OF USER RAM
23FF             22 TPRAM    EQU     BTRAM+3FFH      ;TOP OF USER RAM
                 23 ;
                 24 ;*******************************************************************************
                 25 ;*                                                                             *
                 26 ;*                          PORT ADDRESSES                                     *
                 27 ;*                                                                             *
                 28 ;*******************************************************************************
                 29 ;
                 30 ;
                 31 ;************************************ SBC *************************************
                 32 ;
0000             33 MODEM    EQU     00H             ;MODEM CONTROL PORT ADDRESS
0003             34 MCNTRL   EQU     03H             ;SBC 8255A CONTROL WORD PORT ADDRESS
                 35 ;
                 36 ;
                 37 ;******************************** OPTO BOARD 1 ********************************
                 38 ;****** (USED FOR 8 ALARMS AND DIGITAL LEVELS 1 AND 2 MS BCD DIGIT INPUT) *****
                 39 ;
00C9             40 MSALM    EQU     0C9H            ;MS ALARM BYTE PORT ADDRESS
00CA             41 BCD124   EQU     0CAH            ;MS BCD LEVELS DIGIT PORT ADDRESS (INVERTED)
00CB             42 OPTO1    EQU     0CBH            ;CONTROL WORD PORT ADDRESS OF OPTO I/O BOARD 1 8255A
                 43 ;
                 44 ;
                 45 ;******************************** OPTO BOARD 2 ********************************
                 46 ;************* (USED FOR DIGITAL LEVEL 1 BCD'S 0,1,2 AND 3 INPUT) *************
                 47 ;
00D1             48 BCD101   EQU     0D1H            ;LEVEL 1 BCD'S 0 AND 1 PORT ADDRESS
00D2             49 BCD123   EQU     0D2H            ;LEVEL 1 BCD'S 2 AND 3 PORT ADDRESS (INVERTED)
00D3             50 OPTO2    EQU     0D3H            ;CONTROL WORD PORT ADDRESS OF OPTO I/O BOARD 2 8255A
                 51 ;
                 52 ;
                 53 ;******************************** OPTO BOARD 3 ********************************
                 54 ;************ (USED FOR DIGITAL LEVEL 2 BCD'S 0,1,2 AND 3 INPUT) **************
```

```
ISIS-II 8080/8085 MACRO ASSEMBLER, V4.0        MAP     PAGE    2


  LOC  OBJ        LINE        SOURCE STATEMENT

                    55 ;
  00D9              56 BCD201  EQU     0D9H            ;LEVEL 2 BCD'S 0 AND 1 PORT ADDRESS
  00DA              57 BCD223  EQU     0DAH            ;LEVEL 2 BCD'S 2 AND 3 PORT ADDRESS (INVERTED)
  00DB              58 OPTO3   EQU     0DBH            ;CONTROL WORD PORT ADDRESS OF OPTO I/O BOARD 3 8255A
                    59 ;
                    60 ;
                    61 ;******************************** OPTO BOARD 4 ********************************
                    62 ;*************** (USED FOR 2 LS ALARM BITS IF 10 ALARMS REQUIRED) *************
                    63 ;
  00F1              64 LSALM   EQU     0F1H            ;LS ALARM BYTE
  00F3              65 OPTO4   EQU     0F3H            ;CONTROL WORD PORT ADDRESS OF OPTO I/O BOARD 4 8255A
                    66 ;
                    67 ;
                    68 ;********************************** PWT BOARD ***********************************
                    69 ;
  00E0              70 PARM    EQU     0E0H            ;PARAMETER BUG PORT ADDRESS
  00E1              71 STATUS  EQU     0E1H            ;SYSTEM STATUS DISPLAY PORT ADDRESS
  00E2              72 PRTSEL  EQU     0E2H            ;PORT SELECT ADDRESS
  00E3              73 PWT     EQU     0E3H            ;PWT BOARD 8255A CONTROL WORD PORT ADDRESS
  00E4              74 PCNTR0  EQU     0E4H            ;PWT BOARD COUNTER 0 DATA REGISTER PORT ADDRESS
  00E5              75 PCNTR1  EQU     0E5H            ;PWT BOARD COUNTER 1 DATA REGISTER PORT ADDRESS
  00E6              76 PCNTR2  EQU     0E6H            ;PWT BOARD COUNTER 2 DATA REGISTER PORT ADDRESS
  00E7              77 PCNTWD  EQU     0E7H            ;PWT BOARD 8254 CONTROL WORD PORT ADDRESS
  00E8              78 ONESHT  EQU     0E8H            ;PWT BOARD ONE SHOT TRIGGER PORT ADDRESS
                    79                                 ;SAME ADDRESS USED FOR BACKUP WATCHDOG
                    80                                 ;ON POWER MODULE
                    81 ;
                    82 ;
                    83 ;************************* MODEM ************************************************
                    84 ;
  00BC              85 MCNTR0  EQU     0BCH            ;MODEM PIT COUNTER 0
  00BD              86 MCNTR1  EQU     0BDH            ;MODEM PIT COUNTER 1
  00BE              87 MCNTR2  EQU     0BEH            ;MODEM PIT COUNTER 2
  00BF              88 MCNTWD  EQU     0BFH            ;MODEM PIT CONTROL WORD REGISTER
                    89 ;
                    90 ;
                    91 ;************************ A/D BOARD'S ***************************************
                    92 ;
  0083              93 ACNWDP  EQU     83H             ;POSITIVE A/D BOARD PIT CONTROL WORD REGISTER;
  0080              94 ACTR0P  EQU     80H             ;POSITIVE A/D BOARD PIT COUNTER 0 (CONVERTED DATA)
  0081              95 ACTR1P  EQU     81H             ;POSITIVE A/D BOARD PIT COUNTER 1 (CONVERSION TIME)
  0082              96 ACTR2P  EQU     82H             ;POSITIVE A/D BOARD PIT COUNTER 2 (PRESCALER)
  0093              97 ACNWDN  EQU     93H             ;NEGATIVE A/D BOARD PIT CONTROL WORD REGISTER;
  0090              98 ACTR0N  EQU     90H             ;NEGATIVE A/D BOARD PIT COUNTER 0 (CONVERTED DATA)
  0091              99 ACTR1N  EQU     91H             ;NEGATIVE A/D BOARD PIT COUNTER 1 (CONVERSION TIME)
  0092             100 ACTR2N  EQU     92H             ;NEGATIVE A/D BOARD PIT COUNTER 2 (PRESCALER)
  0084             101 STRCNV  EQU     84H             ;COMMON 'START CONVERSION' PORT
  0085             102 CHNSEL  EQU     85H             ;COMMON CHANNEL SELECTOR PORT
                   103 ;
                   104 ;
                   105 ;
                   106         END
```

CHAPTER 4 THE OUTSTATION SOFTWARE

4.1 Introduction

This chapter describes the outstation software in detail. Special attention is paid to those parts of the software which interface directly to the hardware described in Chapter 3 and to those areas where critical timing loops exist. Complete software listings are not included as the writer feels that this is unnecessary for this kind of thesis since the software is not the only aspect of the project. However, short extracts of the program listings are given for those areas mentioned above.

All the software was written in INTEL 8085 Assembler language. This was chosen for three reasons:-

(i) Critical timing loops had to be written in Assembler so that execution time could be controlled.

(ii) Using a high level language such as INTEL's PLM has a code space overhead which was not desirable with the limited EPROM space available on the Single Board Computer. Extra EPROM cards could be installed but this was not considered a good idea in a small system such as this.

(iii) Prior to commencement of the project, the writer had a good working knowledge of the MOTOROLA 6800 Assembler language only, and the same level of familiarity of the 8085 Assembler was sought as it is a very different machine to the former.

An INTEL Microcomputer Development System Series II Model 230 with the INTEL 8085 In Circuit Emulator was used for all the software and hardware development and testing.

4.2 Overall concept

The outstation software consists of a continuously looping low priority routine, called the BACKGROUND TASK which may be interrrupte by any of three higher priority interrupt routines. These are the RX ROUTINE, TX ROUTINE and 1 SECOND ROUTINE. These interrupt routines are prioritised relative to one another. The four routines ie three interrupt routines plus background task form the frame-work of the overall software concept. Their functions are described briefly here, but these and other routines are dealt with in detail in the appendices.

4.2.1 Rx routine

This interrupt routine is entered when the outstation receives a request word from the master station. It checks the validity of the incoming signal, and if found to be valid, determines which information is required, gets this information ready for transmission back to the master station and issues a request-to-send to the modem.

As request words from the master station are completely asynchronous with any processing in the outstation software (refer paragraph 2.2), ie a request word occurs at any time, the Rx routine has the highest priority of the three interrupt routines.

Refer to Appendix C for a full description of the Rx routine.

4.2.2 Tx routine

This interrupt routine is entered when a clear-to-send comes back from the modem. It clocks the reply word bits out to the modem at 600 Baud as required by the communications protocol described in paragraph 1.5.1. The Tx routine has the next lowest priority from the Rx routine.

Refer to Appendix D for a full description of the Tx routine.

4.2.3 1 Second routine

As its name suggests, this interrupt routine is entered at 1 second intervals and is initiated by a 1 Second interrupt from the PWT hardware module as described in paragraph 3.3 (ii). It does the following:-

(i) Controls the analogue-to-digital converter by reading the value from the currently selected channel, storing this value and selecting the next channel. Recall in paragraph 3.2 the analogue input parameters which are the dam levels in some cases (these are digital at some sites) and the flow rates.

(ii) Integrates the flow rate values by calculating a running total (partial sum) as discussed in paragraph 2.4.1. These values are binary values and are referred to as raw values because they require further processing to a form suitable for the master station as discussed in paragraph 2.4.2.4. This is done by the Background Task.

The 1 Second routine has the lowest priority of the three interrupt routines but the 1 Second interrupt is latched so the routine is executed as soon as either the Rx or Tx routine is finished, should either one have been executing when the 1 Second interrupt occurred. Refer paragraph 3.7.1.1(iii). Whenever the 1 Second routine is being executed, a flag called the SECBUSY flag is set. This is discussed more fully in paragraphs 4.3 and 4.4.

Refer to Appendix F for a full description of the 1 Second routine.

4.2.4 Background Task

This routine converts the raw analogue values and raw integrated flow rate values obtained from the 1 Second routine from binary to BCD format as required by the master station. Refer paragraph 2.4.2.

Refer to Appendix I for a full description of the Background Task.

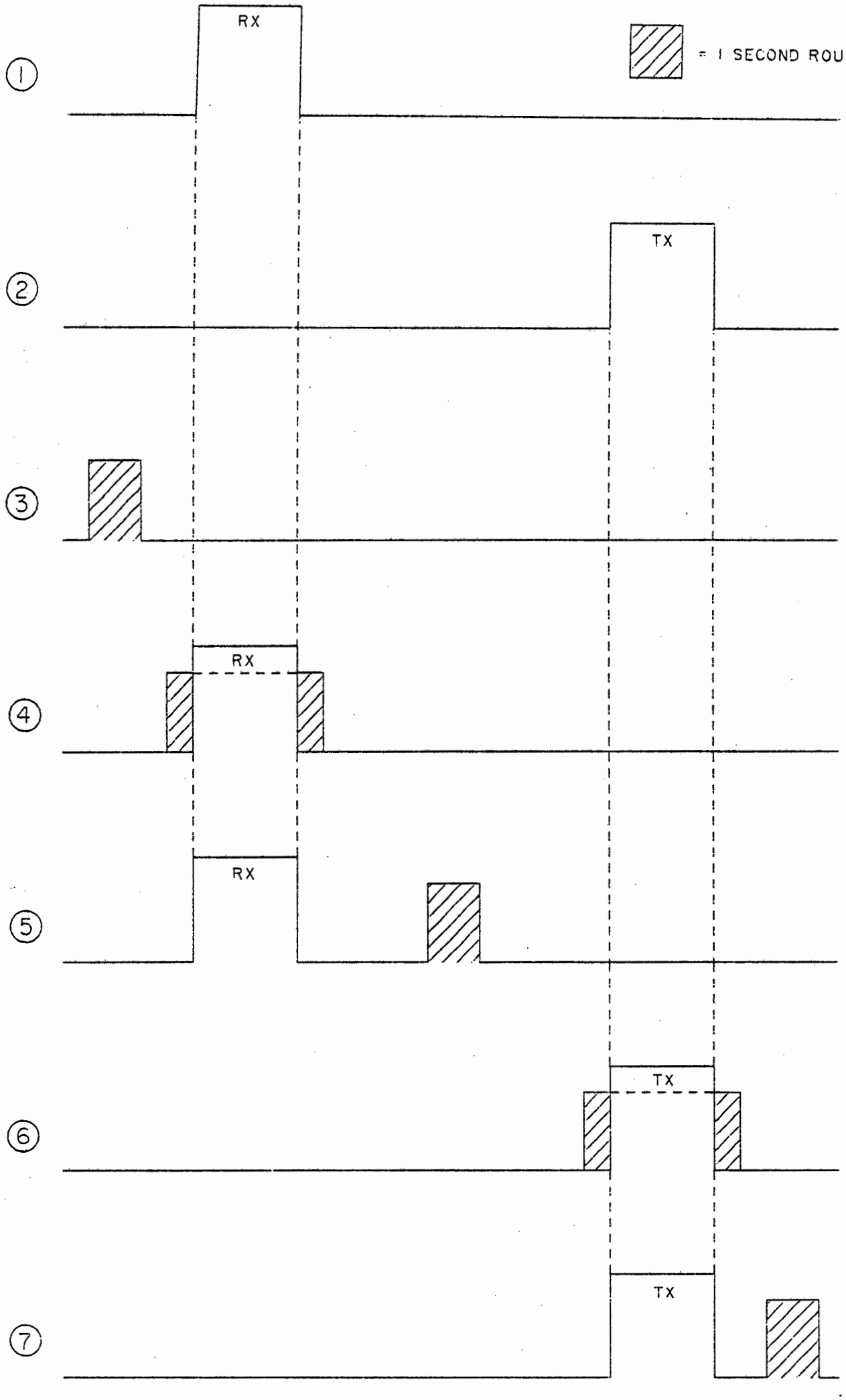
4.3 Interrupt routine interaction

Fig 4.1 illustrates all the possibilities that can occur. Lines 1 and 2 show the relationship between the Rx and Tx routines ie a request from the master station followed by a reply from the outstation. Lines 3, 5 and 7 show the 1 Second routine occurring either before the Rx routine, between the Rx and Tx routines or after the Tx routine respectively. In these cases, there is no interaction between the 1 Second and the Rx or Tx routines. Lines 4 amd 6, however, demonstrate how either the Rx or Tx routines respectively can interrupt the 1 Second routine due to their higher priorities. Note under normal circumstsnces, the Rx and Tx routines would never interact due to the orderly sequence of request from the master station followed by reply from the outstation. Underlying all these interactions, the Background Task is being executed during those periods when the Rx, Tx or 1 Second routine is not.

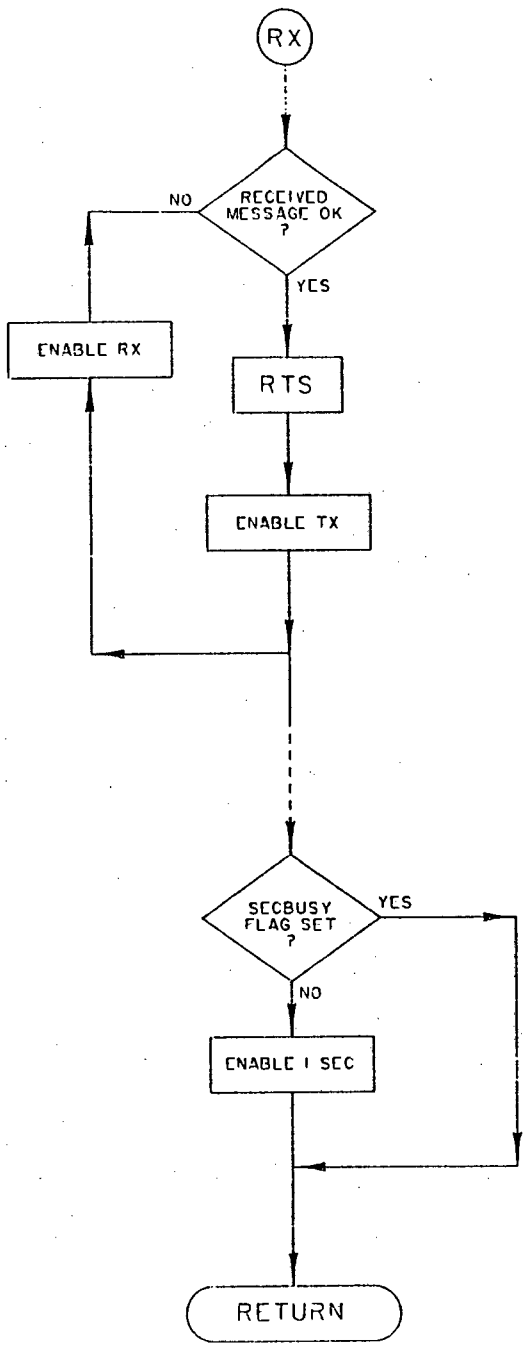
Fig 4.2 shows the logic required in the three interrupt routines to achieve the interaction just described. The following points should be noted:-

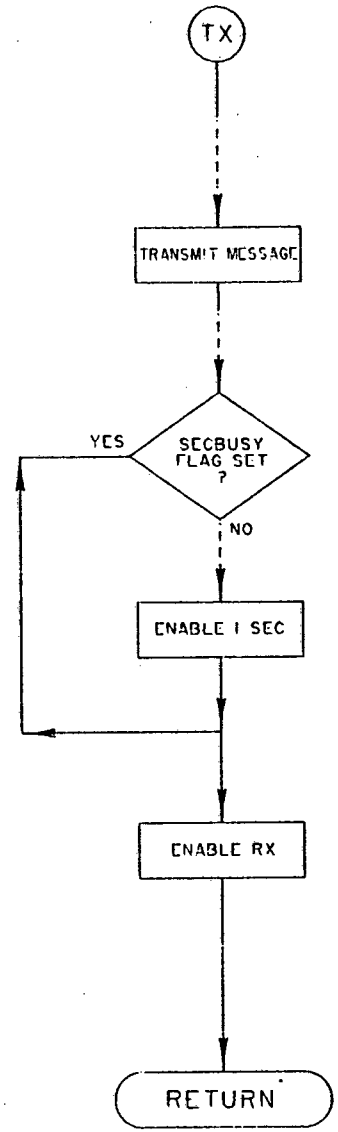
(i) The SECBUSY flag (refer paragraph 4.4) which is controlled by the 1 Second routine is polled by the Rx and Tx routines. If it is set, then this means that the 1 Second routine was interrupted by either of the higher priority Rx or Tx routines and on completion of either of these, execution of the 1 Second routine should be resumed. Refer to Fig 4.1 lines 4 and 6. If the SECBUSY flag is clear, then on completion of either the Rx or Tx routines, execution of the Background Task is resumed.

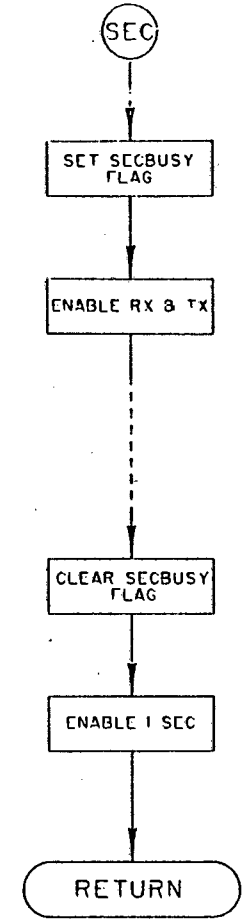
(ii) If the Rx routine receives an invalid message, the Rx routine is re-enabled since no reply is sent back. If the Rx routine receives a valid message, however, then an RTS (request-to-send) is sent to the modem and only the Tx routine is enabled and not the Rx routine. The Rx routine is only re-enabled at the end of the Tx routine initiated by the CTS (clear-to-send) back from the modem as a result of the original RTS from the Rx routine referred to above. This means that should



INTERRUPT ROUTINE INTERACTION | FIG 4.1







INTERRUPT ENABLE LOGIC

FIG 4.2

the CTS back from the modem not initiate a Tx routine due to a hardware fault, then the Rx routine is permanently disabled and that outstation is off-line since it can no longer receive request words from the master station. This may be seen as a fail-safe feature.

Refer paragraph 2.2 for more details of the outstation/modem control.

4.4 Important flags, buffers and counters

The name of the flag, buffer or counter, where applicable, is followed by the name of the software module in which it is defined in brackets. Only the most important of these are listed.

INFLAG (INIT) 'Initialisation in progress' flag
Controlled by the Initialisation routine and polled by the Background Task; when set, the Background Task is treated as a subroutine used to establish an initial memory image before the outstation replies - this only occurs during initialisation; when the flag is clear, the Background Task runs in a loop.

SECB (SEC) '1 Second interrupt in progress' flag (SECBUSY flag)
Set at the beginning of and cleared at the end of the 1 Second interrupt. Polled at the end of the Rx and Tx routines; if set, program execution is resumed in the 1 Second routine - if clear, program execution is resumed in the Background Task.

ALTSEC (SEC) Alternate second flag
Toggled at the beginning of the 1 Second routine; if set, the 1 Second routine is executed; if clear, the 1 Second routine is almost completely bypassed.

CNTRL (BACK) BCD buffer control flag
Toggled on each loop of the Background Task; when cleared, the main BCD buffers for levels, flow rates and integrated flow rates are accessed; when set, the mirror BCD buffers are accessed.
Refer to DBUFF (BACK) below.

START0 (RX) Receive buffer

46-byte buffer which accomodates a double message (ie status output request word as described in paragraph 1.5.3); it has partitions at:-

OSAD	(outstation address	5 bytes)
PTAD	(point address	7 bytes)
FCTN	(function code	4 bytes)
PBUFF0	(first message parity code	5 bytes)
STOP0	(first stop bit	1 byte)
START1	(second start bit	1 byte)
DATA	(second message data	16 bytes)
PBUFF1	(second message parity code	5 bytes)
STOP1	(second stop bit	1 byte)

STRTX (TX) Transmit buffer

23-byte buffer for reply words; it has partitions at:

DATATX	(Tx data	16 bytes)
PARTX	(Tx parity code	5 bytes
STPTX	(Tx stop bit	1 byte)

RAWALV (SEC) Raw analogue level buffer

4-byte buffer for 2 X 16-bit raw binary level values direct from the A/D converter.

RAWALFL (SEC) Raw analogue flow rate buffer

16-byte buffer for 8 X 16-bit raw binary flow rate values direct from the A/D converter.

TOTAL (SEC) Partial sum buffer

12-byte buffer for 3 X 32-bit raw binary partial sums calculated by adding the selected raw flow rate values to the current total every alternate second (refer ALTSEC flag above).

DIV (SEC) Divisor buffer

3-byte buffer containing the number of flow rates of which each of the respective integrated flow rates is a function; written into by the 1 Second routine and read by the Background Task.

LVLBASE (BACK) BCD level buffer
8-byte buffer for 2 X 5-digit BCD levels. Refer to Fig 4.3(a).

FLBASE (BACK) BCD flow rate buffer
16-byte buffer for 8 X 3-digit BCD flow rates. Refer to Fig 4.3(b).

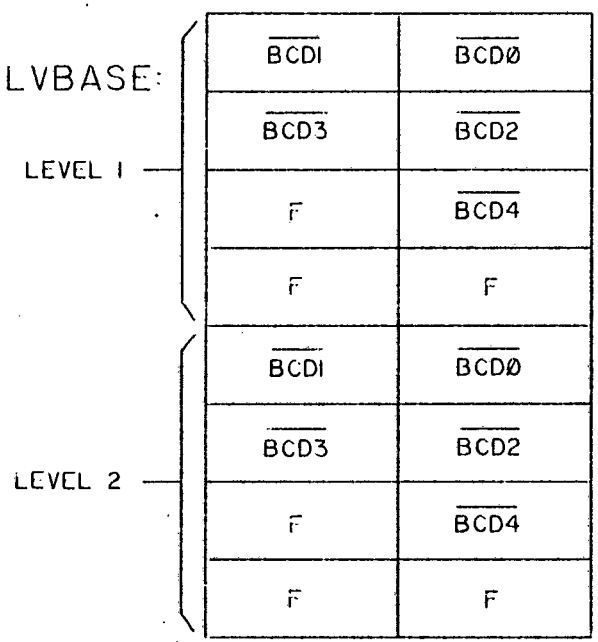
IFBASE (BACK) BCD integrated flow rate buffer
12-byte buffer for 3 X 6-digit integrated flow rates. Refer to Fig 4.3(c).

DBUFF (BACK) Mirror buffer for BCD levels, flow rates and integrated flow rates

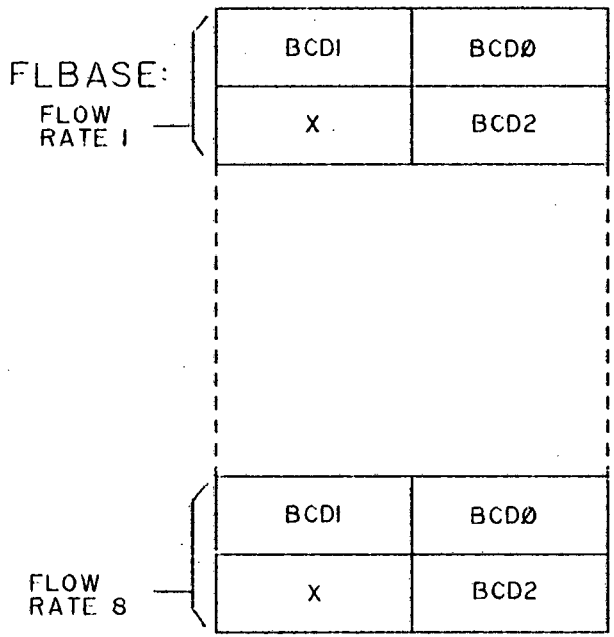
The buffers for BCD levels, flow rates and integrated flow rates are repeated so that the Background Task updates one buffer while the other is available for reply words; this is to prevent the possibility of partially updated information being sent back to the master station which could happen when the Rx routine interrupts the Background Task. The buffer that is accessed is determined by the CNTRL flag already described.

MESP (PACK) Packed message word
Used mainly for 16-bit data content of reply words (bits 1 to 16, refer to Fig 1.5); when so used, the software module UNPACK unpacks this word MS to LS bit into 16 consecutive bytes starting at DATATX; also used by the software module PACK which packs the most significant bits of consecutive bytes in a direction of LS bit of MESP to MS bit of MESP+1.

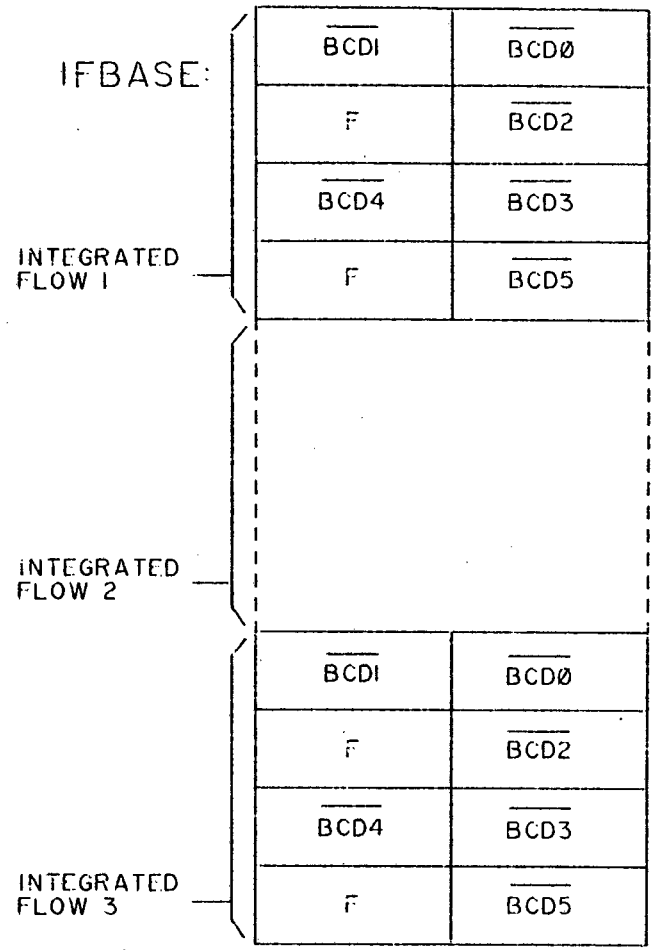
DELAY (DELAY) Delay loop counter
Delay loop used to synchronize the Rx and Tx data rates to 600 Baud. Refer to Appendix E.



a. LEVELS



b. FLOW RATES



c. INTEGRATED FLOW RATES

BCD BUFFERS

FIG 4.3

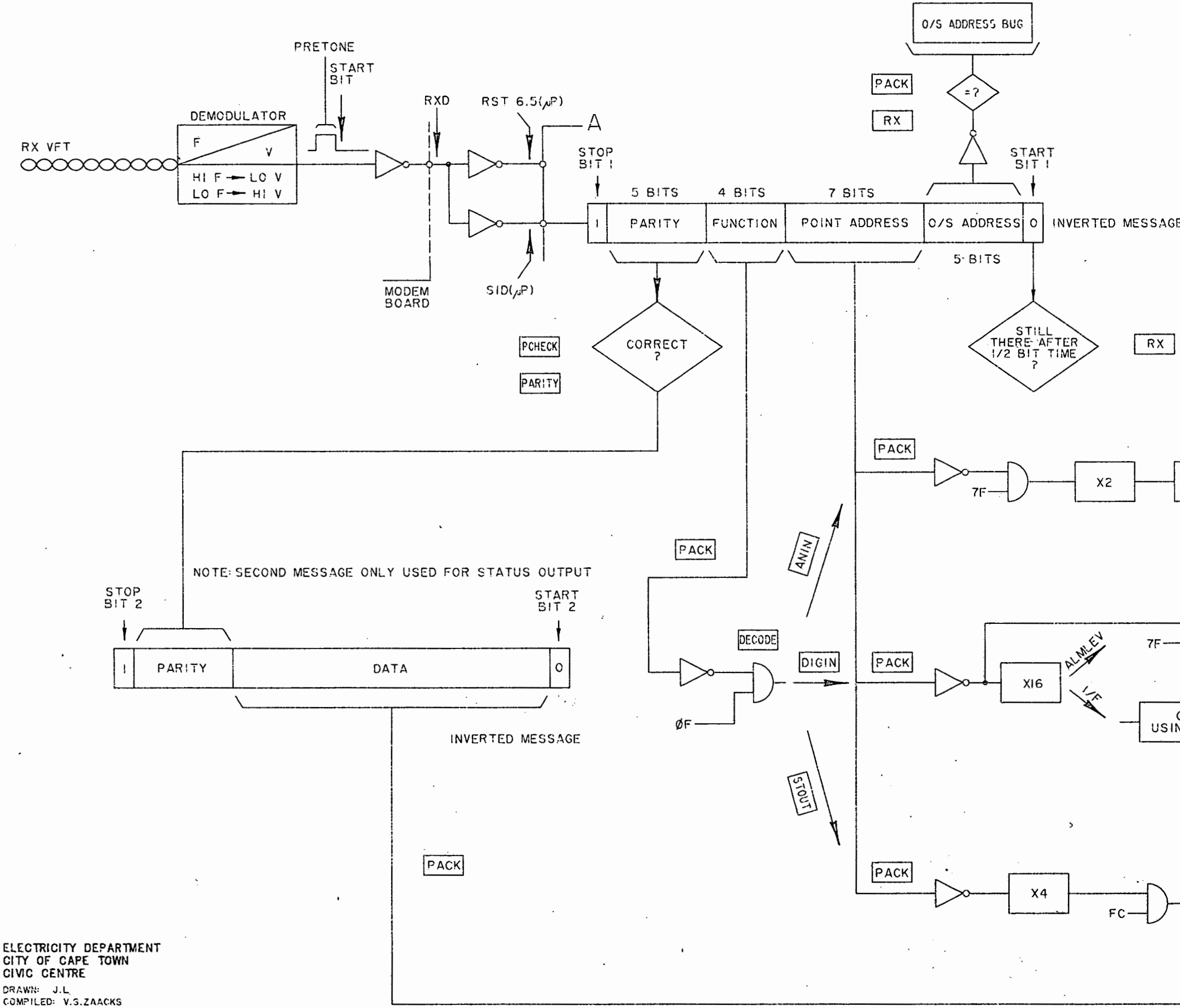
4.5 Message processing

Fig 4.4 is a complete information processing diagram from the Rx VFT signal from the request word to the Tx VFT signal of the reply word; it explains how the request word is analysed and the reply word is synthesised. Note that Fig 4.4 is neither a flow chart nor a logic diagram; it is a schematic aid in describing the information processing in the outstation. All processing inside the boundary lines A-A is done with software, all processing outside these boundaries is done with hardware.

To illustrate the use of this diagram an example will be worked through. The integrated flow rate polling sequence described in paragraph 1.5.3.4 (i) to (vi) will be dealt with as this is the most involved sequence and will make maximum use of the diagram.

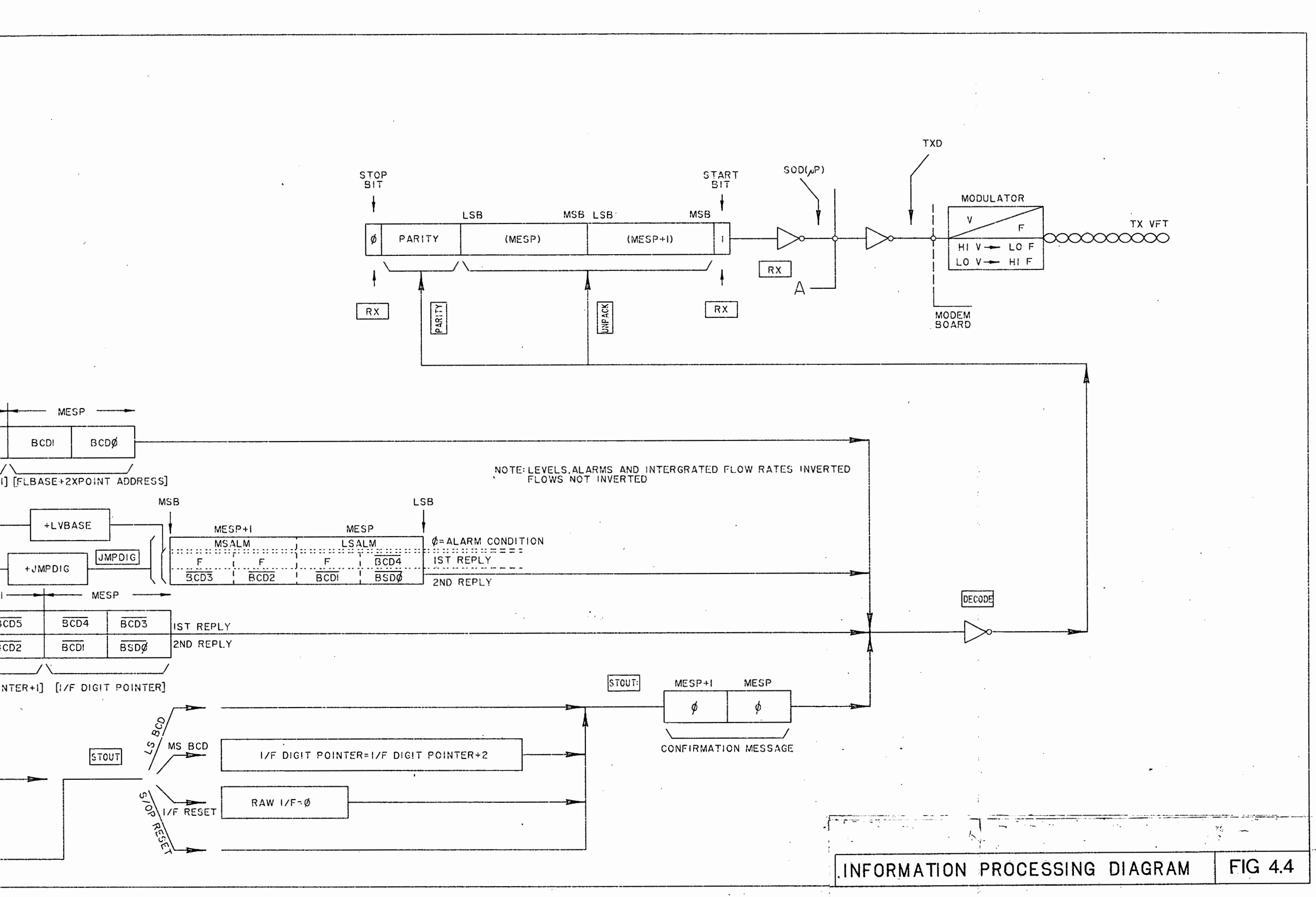
The pretone of the request word from the master station is 1300Hz as mentioned in paragraph 1.5.2(iii); the demodulator output goes high generating an Rx interrupt via two hardware inverters. After the pretone, the start bit arrives and its validity is checked by Rx routine (shown in a block). The status output request word is a double message, so 46 bits are clocked in. The routines PCHECK and PARITY are used to check the parity of the double message. PACK and RX check that the outstation address is correct. DECODE then decodes the function bits and in this case branches to the module STOUT (for status output). PACK then packs the point address and the result is multiplied by 4 (since 4 bytes per integrated flow rate are required) and adds the result to IFBASE, the base address of the integrated flow rate BCD buffer (refer to Fig 4.3(c)). This result is stored in the integrated flow rate digit pointer and is pointing to the LS BCD digits of the integrated flow rate in question. STOUT takes the data content of the second message and four possibilities are catered for ie:-

select MS BCD digits of integrated flow rate
OR select LS BCD digits of integrated flow rate
OR reset integrated flow rate
OR reset status output bits to zero (refer paragraph 1.5.3.4 and Fig 1.4).



ELECTRICITY DEPARTMENT
CITY OF CAPE TOWN
CIVIC CENTRE

DRAWN: J.L.
COMPILED: V.S.ZAACKS
INFO.
CHECKED:



INFORMATION PROCESSING DIAGRAM | FIG 4.4

As this is the first status output word of the polling sequence for the integrated flow rate in question, the MS BCD digits are required so that the integrated flow rate digit pointer is incremented by 2 to point to the MS BCD digits (refer to Fig 4.3(c)). STOUT puts the all-zero confirmation message in the packed message word MESP which is inverted by DECODE and then unpacked into the Tx buffer by UNPACK PARITY generates the parity bits and TX clocks the message out to the modem when the CTS comes back to it.

The second request word is a digital input message as explained in paragraph 1.5.3.4 (i) to (vi). The processing is the same up to the branch where DECODE decodes the function code which is now digital input. DIGIN interrogates bit 8 of the request word (refer to Fig 1.4 and as it is zero in this case, the integrated flow rate branch is taken. The integrated flow rate digit pointer which was set up by the previous status output request word is used to access the required BCD digits of the integrated flow rate in question, in this case the MS BCD digits. The rest of the process is the same as before.

The third request word is a status output like the first one and the only processing difference is that the integrated flow rate pointer is not incremented by 2 but left pointing at the LS BCD digits of the integrated flow rate.

The fourth request word is a digital input message like the second one with identical processing, but this time accessing the LS BCD digits of the integrated flow rate in question.

The fifth request word is a status output like the first one with identical processing except that the raw integrated flow rate is reset to zero.

The sixth request word is a status output the same as the fifth but no software action is necessary as regards accessing any data since this is the status output card reset case which only affects the older TELEPACE hardware-only outstations. The software merely complies with the existing polling sequence as mentioned in paragraph 1.5.3.4 (i) to (vi).

The processing for all other request words is along similar lines as described above only simpler since each request word is a single message and requires only one reply word.

Throughout Fig 4.4, logic symbols in the software section of the processing represent the logical operations which are perforemed at various stages eg after the function code is packed by PACK, DECODE inverts the result and strips off the most significant four bits by ANDing with 0F and then branches either to ANIN, DIGIN or STOUT depending on the function code. Notice that all parts of the received request word are inverted except for parity as mentioned in paragraph 1.5.3. Fig 4.4 illustrates this quite concisely.

4.6 Utility routines

The outstation software consists of twenty-four modules. The main four have already been described in paragraph 4.2; these form the software kernel. The remaining twenty are functional utility routines required by the kernel. These will now be described in outline. Where necessary, a more detailed treatment is given in an appendix, to which the reader will be referred.

4.6.1 INIT: Initialisation routine

This routine is only executed once after:-

(i) A power-up reset.

(ii) A manually applied reset on the pushbutton on the front plate of the SBC.

(iii) A reset originating from either the soft or hard watchdog timers (refer paragraph 2.5).

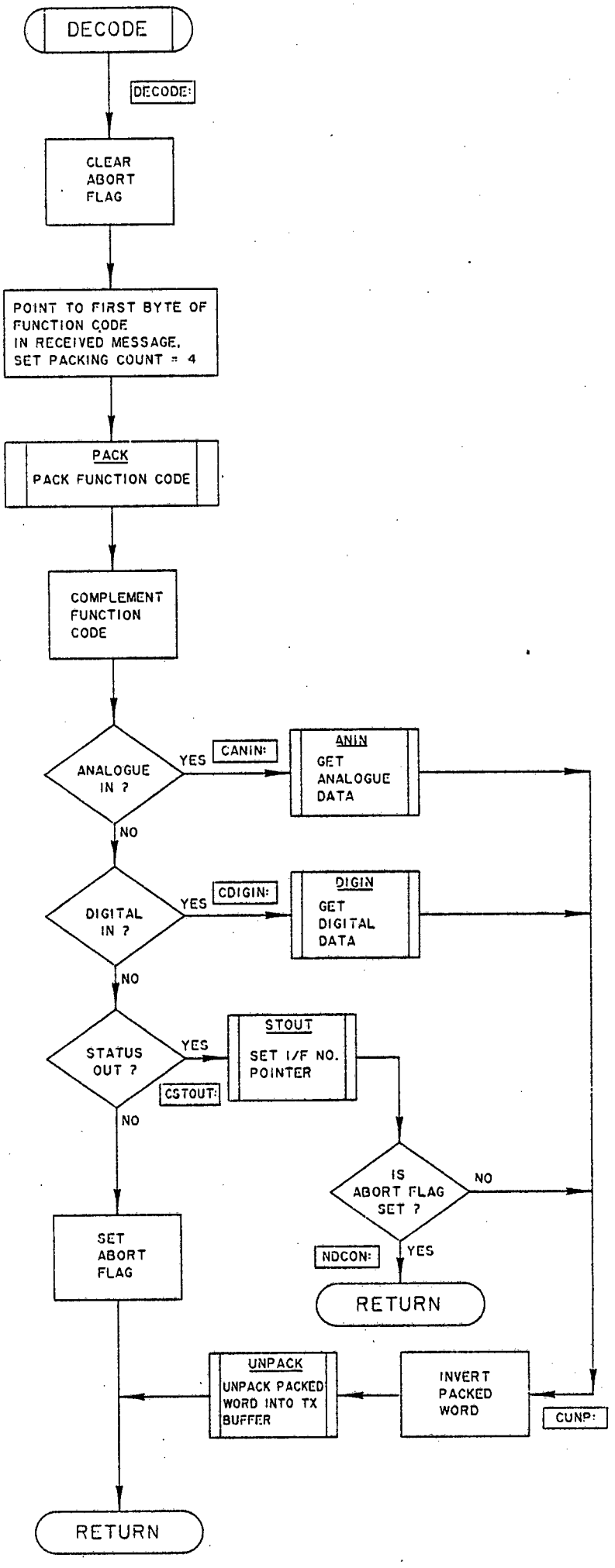
It initialises all the hardware on the SBC, PWT, A/D and MODEM modules. While it is being executed, the 'RESTART' LED on the PWT module is on. Refer to Appendix J for a full description of the Initialisation routine.

4.6.2 DECODE: Function code decoder routine

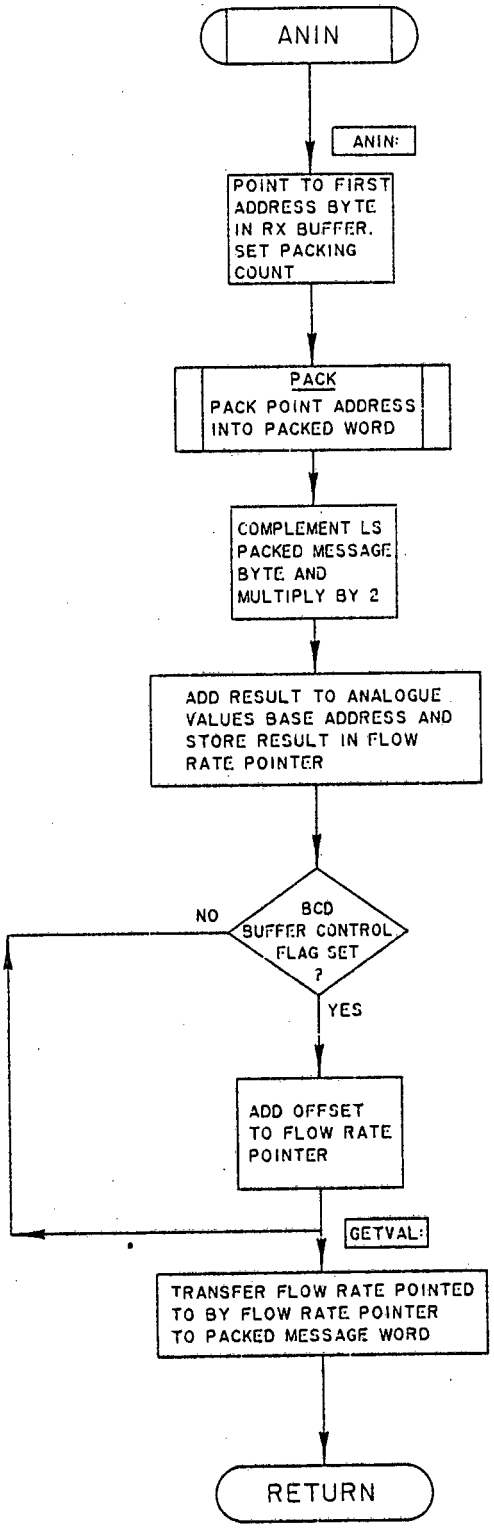
Refer to the simplified flow chart in Fig 4.5. This routine examines the function code of the request word and calls one of the relevant subroutines ANIN, DIGIN or STOUT for analogue input, digital input or status output functions respectively; if the function code is none of these then it is an invalid code and the abort flag FABORT is set, which is interrogated by the Rx routine; if STOUT is called and the data of the second part of the double message is invalid, then FABORT is also set by STOUT. (Refer to Appendix C for interrogation of FABORT).

4.6.3 ANIN: Analogue input routine

Refer to Fig 4.6. This routine uses the point address of the request word to obtain the required flow rate; this is done quite simply by multiplying the point address by two since there



FUNCTION CODE DECODER ROUTINE | FIG 4.5



ANALOGUE INPUT ROUTINE | FIG 4.6

are two bytes required for each BCD flow rate (refer to Fig 4.3(b)) and adding the result to FLBASE, the base address of the BCD flow rate buffer. Notice that the BCD buffer control flag, CNTRL, is interrogated, and if set, the offset discussed in Appendix I is added to the above result so the mirror buffer is accessed while BACK is updating the FLBASE buffer and vise versa. (Refer to DBUFF in paragraph 4.4). The required flow rate is then transferred to the packed message word MESP.

4.6.4 DIGIN: Digital input routine

This routine determines whether an alarm, level or integrated flow rate is requested. In the case of levels, it determines whether the levels are read from the A/D module or digital I/O module ie analogue or digital levels by interrogating switch 8 of switch bank A of the PWT module (refer paragraph 3.7.2.1). Since levels require two request/reply sequences, DIGIN determines from the point address in the request word which digits of a particular level are required. Refer paragraph 1.5.3.2.

For integrated flow rates, DIGIN fetches the digits indicated by a digit pointer which was set up by STOUT after the status output request word immediately prior to this integrated flow rate request word.

Refer to Appendix K for a full description of the digital input routine.

4.6.5 JMPDIG: Digital input routines

This is a suite of digital input routines, each starting on a sixteen byte boundary. There is one alarm input routine and two digital level pair input routines ie five in all. In the alarm routine, the six least significant bits of the alarm word are set to 0. As mentioned in paragraph 1.5.3.1 this is essential to prevent master station programme stoppages; the reason for this is unknown. The input routine that is entered is determined in the digital input routine and the sixteen byte boundaries for which these input routines commence is the reason that the level/alarm request word point address is multiplied by sixteen in the digital input routine as discussed in Appendix K.

4.6.6 STOUT: Status output routine

This routine either determines from the point address in the status output request word the integrated flow rate digits to be transmitted following the next digital input request word, or it resets the indicated integrated flow rate (refer paragraph 1.5.3.4(i) to (vi) and 4.6.4). In both cases it prepares a confirmation reply word.

Refer to Appendix L for a full description of the status output routine.

4.6.7 PACK: Pack routine

This packs the MS bits of sixteen consecutive bytes into MESP (refer paragraph 4.4).

4.6.8 UNPACK: Unpack routine

This unpacks the sixteen bits in MESP (refer paragraph 4.4) into sixteen consecutive bytes; if the bit in MESP is '1' then the unpacked byte is set to FF and if the bit is '0' then the unpacked byte is set to 00.

4.6.9 PARITY: Parity routine

This routine is a software simulation of the parity generator described in Appendix B; given the sixteen data input bits, it generates the five parity bits. These bits are the MS bits of consecutive bytes in the Rx buffer START0 (refer paragraph 4.4).

4.6.10 PCHECK: Parity check routine

This routine checks the received message's parity and indicates to the Rx routine whether it is correct or not.

4.6.11 COMP16: Sixteen bit comparison routine

This routine checks for equality between two sixteen bit words.

4.6.12 DELAY: Delay routine

This routine is a software delay and is used extensively in the Rx routine for serial data input strobing and debouncing. It is also used in the Tx routine for serial data output strobing. All data strobing is at 600 Baud. This is described fully in Appendix E.

4.6.13 BCD: Binary-to-BCD conversion routine

This routine is used for the conversion of the raw analogue levels, flow rates and integrated flow rates in the Background Task. It uses the LOOKUP module (refer paragraph 4.6.14) to get the 5-byte BCD equivalent of each bit in the binary input word and decimally adding these together to form the BCD result.

4.6.14 LOOKUP: BCD lookup-value module

This is a data lookup-table module used by the BCD routine in converting binary values to BCD (refer paragraph 4.6.13).

4.6.15 MULT: Multiply routine

This routine is used extensively in the Background Task for averaging and scaling integrated flow rates. It uses the standard 'shift and add' technique of multiplying two binary numbers together. Refer to Appendix H for more details of its use.

4.6.16 CALC: Calculate routine

This routine adds two 4-byte binary numbers together; it is used in calculating the partial sums for the integrated flow rates in the 1 Second routine.

4.6.17 SHIFTR: Shift-right routine

This routine shifts a 16-bit word one place to the right; it was necessary to write a routine for this because there is no 16-bit shift instruction for the 8085.

4.6.18 SHIFTL: Shift-left routine

As for the SHIFTR routine but opposite direction shifting.

4.6.19 VEC: Vector module

This module contains the jump instructions to the start of TX, RX, 1SEC and INIT. For more information on the interrupt structure of the 8085 the reader is referred to the manual.

4.6.20 MAP: Map module

This is a list of all hardware memory and port mappings and hardware related constants in the outstation software. Refer to paragraph 3.12 for a listing.

CHAPTER 5 CONCLUSION

5.1 What were the problems?

The outstation prototype was tested experimentally in a workshop environment prior to field testing. Initially, it was connected directly to the master station computer by telephone line. It was during this phase that much of the specific information concerning the message protocol and data formats was gleaned; also the unexplained stoppage of the computer when certain alarm word bits were set, as mentioned in paragraph 1.5.3.1!

Under software emulation it was possible to observe the resultant master station teleprinter logs discussed in paragraph 1.3 as a function of outstation replies for the different data types.

The A/D 8254 PIT prescaling problems as discussed in Appendix G were diagnosed and solved. It was at this point that the need for the PWT hardware module became obvious since it was impossible to monitor outstation software performance without it.

Once satisfactory operation via telephone line was achieved, operation via radio was tested. During this phase, many of the problems concerning the control of the u.h.f. radio by the master station (refer paragraph 2.2) came to light. The extremely well-ordered, tight software control necessary in the Rx routine to overcome modem jitter and u.h.f. receiver squelch noise evolved here also.

Underlying all these problems and their associated solutions is the ever-present hardware/software interface situation. In the writer's experience, it is always the front-end of a system that causes the most problems, where internal software has to interface with external hardware with non-deterministic parameters; the squelch noise and the modem jitter mentioned above are perfect examples of this. Indeed, most of the development time was spent in solving these. In sharp contrast to this, the internal data processing used for the data conversions and numerical integrations discussed in paragraph 2.4 caused absolutely no problems at all.

5.2 What are the results?

Once the prototype was fully operational, it was field tested by operating it is parallel with an existing TELEPACE outstation ie both outstations (with different addresses) reading the same transducers and using the same u.h.f. radio transceiver. In this way it was possible to eliminate any common malfunctions such as transducer failure or radio communication problems by comparing the teleprinter logs of the two outstations; hence prototype behaviour could be isolated and observed.

Over a soak-testing period of about a month, no malfunction ocurred; the analogue measureands tracked very closely, in fact. There were the occasional communication failures, but these were common to both outstations and are usually due to radio interference.

The writer therefore concluded that the prototype was working satisfactorily and that production of the units could proceed.

5.3 What are the alternatives?

Having completed the project satisfactorily, the writer notes in hindsight that several aspects could have been done differently.

5.3.1 Hardware alternatives

(i) Instead of adopting a completely modular approach with functionally distinct SABUS modules, a larger single-board dedicated outstation could be produced. The advantage of this is an improvement in reliability due to the elimination of all the SABUS connectors and the front panel interconnections. The obvious disadvantage is the loss of hardware flexibility.

(ii) The CPU could be split up into two processors ie a front end processor and an internal processor. The front end processor performs all the telemetry communications ie modem control, radio/modem handshaking, receive and transmit data bit strobing and timing, and checking and generating parity; the internal processor does all the rest which is decoding of request words, fetching requested data and internal data processing ie numerical integration and data conversions. These two processors would then communicate using a handshake

type philosophy. There would be a greater need for two processors in larger systems, however, since the tasks for this system are still manageable by one processor.

(iii) The TX/RX baud rate generation and timing could all be done with 8254 PIT's instead of using software. The timers would be programmed to interrupt the internal processor when the timing period has elapsed; this would prevent wastage of processor time in non-productive timing loops.

5.3.2 Software alternatives

(i) With the exception of the Tx and Rx routines where timing is critical, the software could have been written in a high level language such as PL/M. When data is stored in arrays as was the case here, data pointers have to be maintained and updated individually by the programmer; this tends to be error prone and much debugging time is used in rectifying errors. High level language compilers, with their in-built array handling capability, maintain all these pointers automatically and are transparent to the programmer. The disadvantage of high-level language compilers is that they generate more code than assemblers for the same program task.

(ii) A small real-time operating system could conceivably have been used. This would take care of all the TX/RX timing, the interrupt prioritising and interaction, and all the I/O operations. Once written, the programmer would no longer have to interweave all these factors with the main task eg the polling of the SECBUSY flag (refer paragraph 4.3) would no longer have to be considered in the Rx and Tx routines; the operating system would take care of this.

5.4 What about the future?

This thesis is open-ended because it has described a particular system within a much broader telemetry environment in which there are many applications within the Cape Town Municipality. All the development work for this project was directly applicable to the Robben Island Radiation Monitor. This consists of a telemetry outstation on Robben Island which measures atmospheric radiation levels and transmits them back to a master station at Cape Town Civic Centre. No new hardware had to be developed for the outstation and only three additional hardware modules for the master station. The outstation software is almost identical to the software described in this thesis, and quite a number of software modules were used in the master station.

There are two further proposed projects:-

(i) A small outstation for the Sewerage Branch of the City Engineer's Department. The single-board approach described in 5.3.1(i) is envisaged here.

(ii) A universal telemetry system which will replace the GEC 2050 master station and another existing TELKOR master station for Sewerage Branch, as well as providing any future requirements. One of these is the telemetry of water pressure values at strategic points in the water supply network; this will enable pipe-bursts to be located more quickly than at present. Another is the provision of remote control facilities eg the opening and closing of valves.

The overall objective of this project is therefore to be able to transmit any analogue or digital value from any point in the Cape Town Municipal area to a central master station and to have remote control facilities in the opposite direction.

Having gained much insight into the problems of telemetry systems, the writer feels well equipped to undertake future projects of this nature.

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APPENDIX A

PRINTOUT FORMATS

This section deals with the printout of information on the two master station teleprinters as a function of reply word information written into the packed message word MESP described in paragraph 4.4. Refer to Fig 1.5

At each outstation, the various points are consecutively numbered from 1 upwards, in the order levels, flow rates, integrated flow rates and alarms. Outputs then follow alphabetically, associated consecutively with the integrated flow rates. (Refer to paragraph 1.5.3.4 where the polling sequence for an integrated flow rate associates a status output point with a digital input point from which the integrated flow rate is read).

For example, for an outstation with 2 levels, 4 flow rates, 3 integrated flow rates and 5 alarms, the points would be identified as follows:-

1L, 2L, 3F, 4F, 5F, 6F, 7I, 8I, 9I, 10A, 11A, 12A, 13A, 14A, O/PA, O/PB, O/PC. Status outputs A,B and C are associated with integrated flow rates 7,8 and 9 respectively. Notice that the alarm points follow on in sequence from the previous points.

Refer to Fig 1.5 for the data format of each type of point.

Levels

5-digit inverted BCD in two consecutive reply words as shown. It was discovered that if hexadecimal numbers A to F are used in the BCD positions, then the master station assigns a decimal weighting to these according to their position and adds up the contribution of each digit to give a total eg 12345 transmitted gives 12.345M on the printout but so too does 1233F; these two values differ in the last two digits but since:

$$4 \times 10 + 5 \times 1 = 45 \text{ and}$$
$$3 \times 10 + 15 \times 1 = 45 \text{ also,}$$

the printout is the same in both cases. Note that 12345 decimal is NOT equal to 1233F hexadecimal! This is a 'decimal coded hex' philosophy which applies to all the digit positions. This type of encoding has never been encountered by the writer before.

If the decimal equivalent of the transmitted value exceeds 65536, then this is first subtracted from the value and the printout 'wraps around' ie:

PRINTOUT = VALUE - 65536 for values greater than 65535.

There is one exception, when the value = 65535 decimal, in which case question marks are printed out.

This behaviour is obviously related to the fact that the master station is a binary machine programmed to work with decimal numbers in some cases; this is indicated very strongly by the 'wrap around' behaviour about the value of 65535 which has a hexadecimal value of FFFF ie the maximum 16-bit number possible. (The master station is a 16-bit machine).

The use of hexadecimal digits for the BCD values is obviously not recommended and hence the software uses BCD format.

Flow rates

3-digit BCD as shown. The same 'decimal coded hex' philosophy as for levels applies. At the master station, these values can be scaled by a multiplier X and a divisor Y and an offset Z can be added to accomodate the transducer gain factor and any offset (a very common transducer operating range is 4 to 20 mA).
So,

PRINTED VALUE = RECEIVED VALUE x X/Y - Z.

If X = Y = 1 and Z = 0 then 0 to 999 in MESP gives a corresponding printout of 0 to 999 ML/D.

Integrated flow rates

6-digit inverted BCD in two reply words as shown. The same 'decimal coded hex' philosophy as for levels and flow rates applies. General printout format is BCD5 BCD4 BCD3 . BCD2 ML. Note that BCD1 and BCD0 are ignored.

Alarms

The most significant ten bits of the alarm word in MESP are used. Note that the least significant six bits MUST be zero as explained in paragraph 1.5.3.1. The alarms are numbered from the most significant bit downwards and the numbering follows on from the other points at that particular outstation as mentioned earlier. The sense is as follows:

1 to 0 bit transition = 'xxxx(n+k)A FAIL' printed out
0 to 1 bit transition = 'xxxx(n+k)A OK' printed out

where n = highest point number of
all other points so far + 1
and k = 0 to L-1 where L is the number of alarm points
at outstation xxxx.

Refer to Fig A1 for sample printouts obtained from the master station teleprinters.

```
18-06-86      11-59
TYBG  1  L                  0.050M
TYBG  2  L                  9.970M
TYBG  3  F                    165ML/D
PLKF  1  F                    114ML/D
PLKF  3  L                 11.599M
VOEL  1  F                      0ML/D
WMHK  1  F                    235ML/D
WMHK  3  L     INHB     ????
```

TIMED LOG OFF ALL SELECTED OUTSTATIONS. NOTICE WEMMERSHOEK 3L INHIBITED.

```
26-06-86      12-04
CNEK  1  L                 25.600M
CNEK  2  F                    281ML/D
CNEK  3  F                      1ML/D
CNEK  4  F                      1ML/D
CNEK  5  F     INHB     ????
```

ON-DEMAND LOG FOR CONSTANTIA NEK. NOTICE THAT 5F IS INHIBITED.

```
18-06-86      12-56
****MOLT  1  L      TIME

18-06-86      12-57
****MOLT  1  L       ON
```

SPONTANEOUS POINT ALARM FOR MOLTENO 1L DUE TO NO REPLY FOR THAT POINT.

```
19-06-86      10-48
****NWLD  2  L      PRTY

19-06-86      10-49
****NWLD  2  L       ON
```

SPONTANEOUS ALARM DUE TO PARITY FAILURE OF THE NEWLANDS 2L POINT.

```
****KILD  1  L      HIGH

30-06-86      15-02
****KILD  1  L       OK
```

SPONTANEOUS HIGH WATER LEVEL ALARM FOR KILDARE ROAD 1L.

FIG A1 SAMPLE PRINTOUTS OF MASTER STATION TELEPRINTER

APPENDIX B

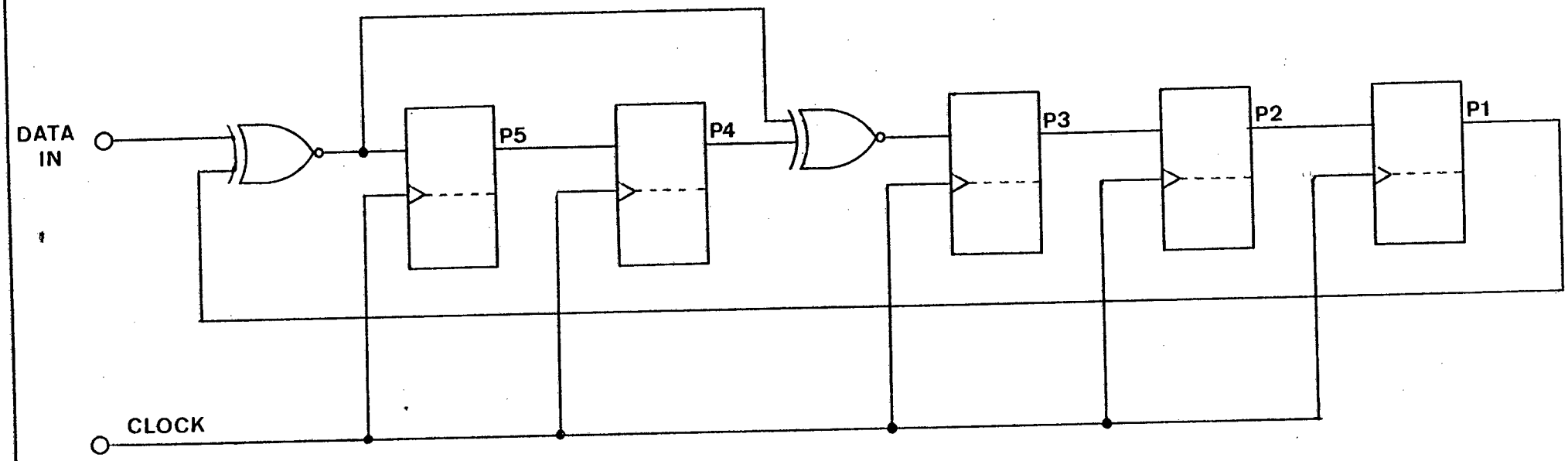
PARITY CODE USED FOR MESSAGE INTEGRITY [3]

The parity code used for data integrity in the Waterworks Telemetry System can be generated by the parity circuit shown in Fig B1. The most significant parity bit (P1) is transmitted immediately following the least significant data bit. The circuit is clocked every time a new data bit is presented to the input. This causes the current parity code to shift one place to the right ie in the direction P5 to P1. Parity bit P1 is compared with the current data bit and if different a '1' bit is shifted into the P5 position. The input of the P5 store is also compared with the P4 store and the result clocked into the P3 store.

The parity code may be considered as the coefficients of a polynomial in the dummy variable x. For example 11010 is represented by the polynomial $1 + x + x^3$. The polynomial is written low-order to high order because these polynomials will be transmitted serially, high order first, and it is conventional to indicate signal flow as occurring from left to right.

The data bits may also be considered as coefficients of a polynomial. This polynomial is multiplied by x^5 by adding 5 parity bits to the low order end. The parity generator divides the data polynomial by $1 + x^2 + x^5$ leaving the remainder in the parity stores. This remainder is then transmitted immediately following the data. As addition and subtraction are identical in modulo two arithmetic, the addition of the remainder makes the whole polynomial exactly divisable by $1 + x^2 + x^5$.

At the receiving end the whole operation is repeated and provided no errors have occurred, the received polynomial (data + parity) will divide exactly by $1 + x^2 + x^5$, and all the parity bits will be zero.



PARITY GENERATOR CIRCUIT

FIG B1

Note that before the message is put through the parity generator, an imaginary '1' bit is clocked into it first. Note also that the stop bit plays no part in the parity generation at all.

The outstation software simulates the circuit of Fig B1.

This parity code gives 100% detection of all 1 and 2 bit errors and error bursts of up to 5 bits and better than 96% for all other bit error combinations.

Although this appears impressive at first, the above figures can be deceptive. This identical parity code was initially used for the Robben Island Radiation Monitor project but was found to be inadequate. The above project is a high security installation where data integrity is essential ie a radiation level alarm can initiate a sequence of events from the Cape Town Civil Defence Unit.

Over a period of 30 days with the outstation being polled at 1 second intervals

ie 30 X 24 X 60 X 60 = 2 592 000 polling sequences

58 spurious radiation alarms were recorded. This represents a failure rate of:-

(58 / 2 592 000) X 100 = 0.0022%

which is well within the 4% failure rate implied by the figure of 96% mentioned above.

To alleviate the problem, the request word/reply word protocol was modified to send twin messages both ways ie a second identical bit stream is appended to each message thereby doubling its length (100% redundancy). The original parity scheme for each message is still retained. If the twin messages are not identical, the message is rejected and a retry sequence is initiated.

The modified system has been running for a month and so far, not one spurious alarm has ocurred. Thus a much lower error rate has been achieved, but at the expense of more security bits. Before, if start and stop bits are excluded, the security bits occupied:-

$$5/21 \times 100 = 23.81\% \text{ of the message.}$$

Now, they occupy:-

$$26/42 \times 100 = 61.90\% \text{ of the message}$$

ie more security bits than information bits.

The above solution was implemented from a practical rather than a theoretical standpoint because the nature of the interference encountered in this instance is man-made. The Cape Town Civil Defence Unit operates many emergency services on radio channels which are in some cases adjacent to the one used for this system; the interference that is sometimes caused is only occasional but usually produces bursts of errors which are so overwhelming (often up to 15 seconds' duration) that no amount of error correction will help. Generally, these effects are not readily quantifiable but are apt to be a major source of errors in systems in the field.[4]

APPENDIX C

RECEIVE INTERRUPT ROUTINE (RX)

Refer to Fig C1 for a simplified flow chart. When the pretone of the request word from the master station is demodulated by the modem in the outstation, the data output RXD of the modem goes low and generates an interrupt on the RST 6.5 input line to the CPU. This causes the Rx routine to be entered. The 'RX' LED is switched on, the 'B/GRND' LED is switched off, together with the 'PRTY FAIL' in case it was switched on due to a parity error from a previous pass of the Rx routine (see later). On entering the Rx routine, a debounce period of approximately 3 ms is inserted due to jitter on the RXD output of the modem; 3 ms was determined by observation as being of sufficient duration to allow all jitter to settle. After the debounce period has elapsed, the SID (Serial Input Data) line of the CPU is read again; if it is still high ie the pretone is still on the line, then this is taken as a valid entry into the Rx routine; if it is low, then it is assumed that noise on the RX VFT input to the modem caused a glitch on the RXD line and the Rx routine is aborted.

For a valid pretone the Rx routine then waits until the SID line goes low. This negative edge is used as a timing reference point to which the sampling of the modem RXD line is synchronised. The Rx routine then waits a further half bit time and then samples the line again; if it has gone high, then the start bit is invalid and the Rx routine is aborted; if it is still low then the incoming request word has passed the initial screening process and the byte START0 of the receive buffer is set to 0 (refer paragraph 4.4). The following 22 bits of the request word are then clocked into the receive buffer, each bit being sampled in the middle.

After receiving 23 bits, the outstation address content of the request word is compared with the outstation address as set up on bits 0 to 4 of switch bank A on the PWT module (refer paragraph 3.7.2.1). If they are not the same, then the request word is not intended for this outstation, or there is message corruption

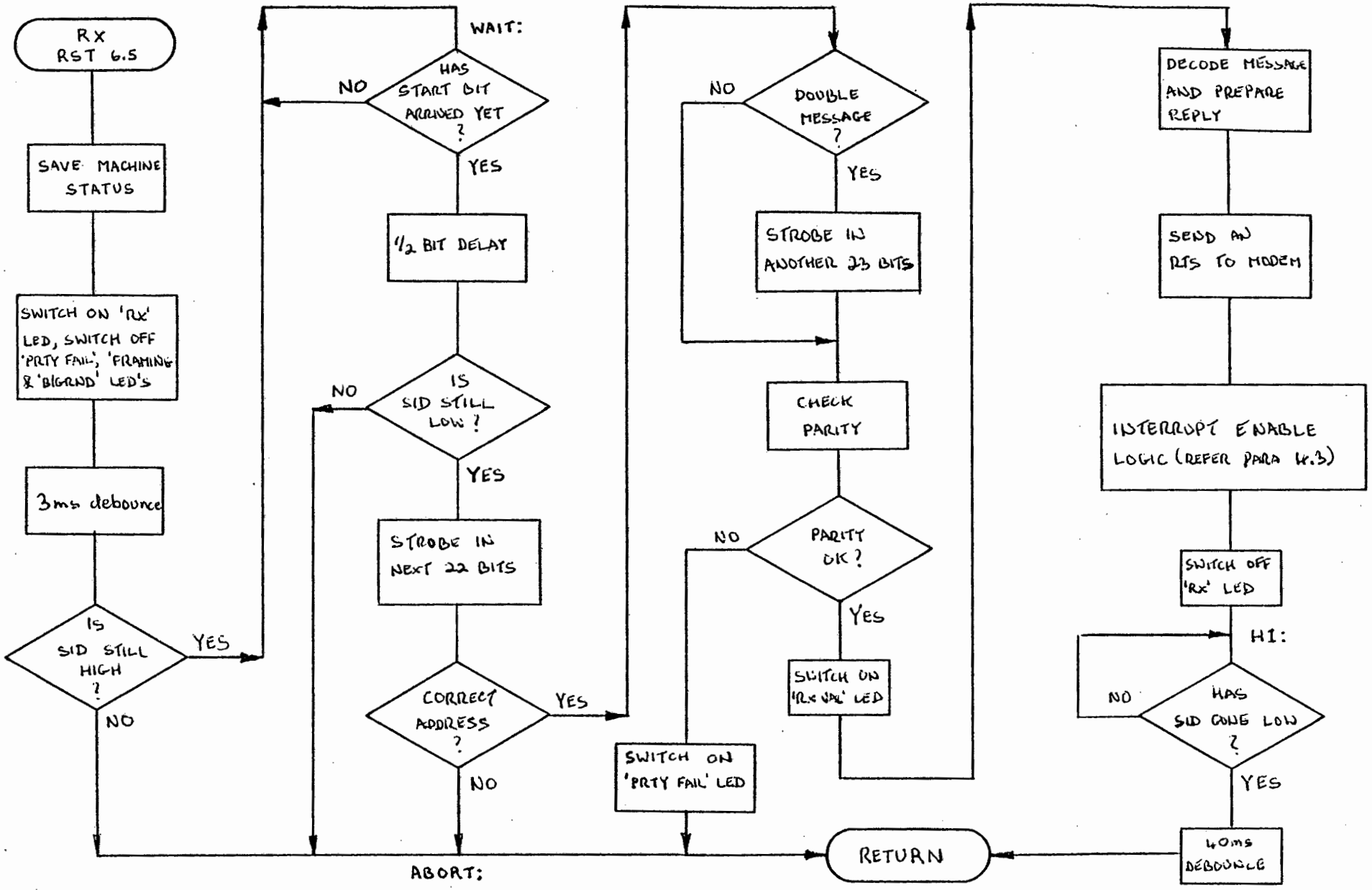


Fig C1 Simplified flow chart of Rx routine

(parity has not been checked yet) and the Rx routine is aborted. If the outstation address is correct then the function code is checked to see if it is a status output request word, in which case a 46 bit double request word is being transmitted and the Rx routine must resynchronise on the second start bit and receive the next 23 bits. A flag FDBMES, the double message flag, is used to control this process.

On receiving the request word, the state of FDBMES determines whether the parity of a single or double message is checked by the routine PCHECK, which sets the parity fail flag FPFAIL if there is a parity error. If this happens, the 'PRTY FAIL' LED is switched on and FPFAIL is reset. If the parity is correct, then the request word is decoded by the routine DECODE which checks the validity of the function code and puts the required data in the transmit buffer bytes DATATX ready for parity generation (refer paragraph 4.4). If DECODE finds that the function code is invalid, then it sets an abort flag, FABORT, which the Rx routine then resets and aborts itself.

Having passed all the tests, the 'RX VAL' LED is switched on and the start and stop bits are written to the transmit buffer bytes STRTX and STPTX (refer paragraph 4.4). The parity bits are then appended to the data bits by the routine PARITY (remember that the start bit plays a part in the parity generation (refer paragraph 1.5.3)) and the whole 23-bit reply word is then inverted for correct logic polarity.

A request-to-send, RTS, signal is then sent to the modem. The RTS/CTS timing of the modem is illustrated by the timing diagram on Fig 3.3.

The double message flag, FDBMES, is then reset; the interrupt enabling logic is explained in paragraph 4.3 with reference to Fig 4.2. The Rx routine then waits for the SID line to go low again and after a debounce period of approximately 40 ms, the 'RX' LED is switched off, and the SECBUSY flag (refer paragraph 4.4) is polled. Again, the interrupt logic has been fully described in paragraph 4.4, and the Rx routine then returns either to the 1 Second routine or the Background Task.

Note that the 40ms debounce period is actually as long as a single message which is

23 X 1.67ms = 38.33ms long.

The reason for this is as follows:-

At the end of a master station transmission its u.h.f. radio transmitter is switched off. At the outstation, its u.h.f receiver detects loss of carrier and its squelch circuit mutes the audio output amplifier. However, this muting is not instantaneous so a short burst of white noise is let through to the outstation modem demodulator. Since white noise contains all frequency components across the entire audio spectrum, the modem demodulator attempts to demodulate it when a frequency component within its passband occurs. This will occur quite randomly since white noise is completely random (it has a Gaussian probabilty density function), and so the RXD line of the modem jitters for the duration of the white noise burst. By observation, this burst can be up to 20 or 30 ms and is at its longest when the request word comes via a repeater as mentioned in paragraph 1.3. This is so because two squelch bursts occur in this case ie one in the receiver at the repeater and one in the outstation receiver. Thus, a 40 ms debounce period allows a safety margin of 10 ms or so. Without this debounce period, the squelch burst would cause the Rx routine to be spuriously re-entered immediately after it has been re-enabled.

Note that the routine DELAY (described in paragraph 4.6.12) and NOP instructions are used to achieve the 3ms and 40ms debounce periods and the synchronising of the input sampling to the middle of the start bit and thereafter at the required 1.67 ms sampling interval for the 600 Baud channel. This is explained fully in Appendix E.

If the 'PRTY FAIL' or 'RX VAL' LED's were switched on during the Rx routine, the Rx routine does not switch them off on completion. The 'PRTY FAIL' LED is switched off at the beginning of the next pass of the Rx routine, while the 'RX VAL' LED is switched off at the start of the Tx routine (refer Appendix D).

The 'B/GRND' LED, which was switched off at the beginning of the Rx routine is not switched on at the end; this is left to the Background Task (refer Appendix I).

APPENDIX D

TRANSMIT INTERRUPT ROUTINE (TX)

Refer to the simplified flow chart of Fig D1. This routine is initiated by the clear-to-send line back from the modem (refer paragraph 4.2.2) generating an interrupt on the RST 5.5 line of the CPU. It first switches on the 'TX' LED and switches off the 'RX VAL' and 'B/GRND' LED's. The 23 bits which were put into the Tx buffer by the Rx routine are then clocked out to the Tx Data (TXD) line of the modem. The 600 Baud timing is achieved in much the same way as in the Rx routine, using the DELAY routine and NOP instructions. This is explained in Appendix E. When all 23 bits have been clocked out, the Tx routine switches the 'TX' LED off and polls the SECBUSY flag (refer paragraph 4.4). The logic which follows concerning the re-enabling of interrupts has been described in full in paragraph 4.3 with reference to Fig 4.2.

Notice that as in the Rx routine, the 'B/GRND' LED is not switched on at the end of the Tx routine; the logic is the same as in the Rx routine.

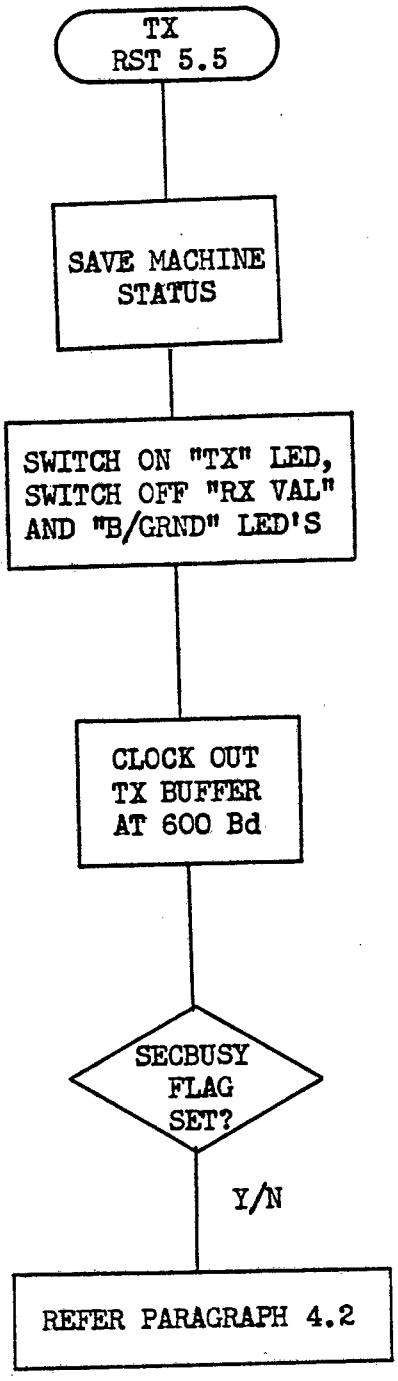


Fig D1 Simplified flow chart of Tx routine

APPENDIX E

SOFTWARE TIMERS

In a few instances in the software, it is important that execution time is controlled. This is done by determining the number of CPU clock cycles used in the instruction sequence.

For this system, the clock frequency is:-

$$f1 = 3.072 \text{ MHz}$$

Therefore, the time duration of a clock cycle is given by:-

$$Tc = 1/3.072 \text{ microseconds}$$
$$= 325.521 \text{ nanoseconds}$$

In the program listings which follow, the numbers in parentheses next to the op-codes indicate the number of 8085 clock cycles used for that instruction; these are obtained from the 8080/8085 ASSEMBLY LANGUAGE PROGRAMMING MANUAL. Note that two numbers are shown next to a jump instruction; the larger of the two indicates the number of clock cycles when the jump is executed and the smaller number when it is not.

Refer to Fig E1 where the DELAY routine referred to in paragraph 4.6.12 is listed. DELAY is called as a subroutine and its execution time is controlled by a 16-bit parameter passed in the BC register pair. It decrements this register until it reaches zero, wherupon DELAY returns to the calling routine.

While the BC register pair is being decremented, the program loop is lines 15 to 18. The clock cycles for one pass of the loop may be determined as follows:-

Line 15		6 clock cycles
" 16		4 " "
" 17		4 " "
" 18 (executed)		10 " "
	TOTAL	24 clock cycles

The execution time of a loop is therefore 24 Tc ns.

```
15 DELAY:   DCX   ( 6) B                    ;EXECUTE DELAY
16          MOV   ( 4) A,B
17          ORA   ( 4) C
18          JNZ(7/10) DELAY
19          RET   (10)                      ;RETURN AT END OF DELAY
```

FIG E1: DELAY ROUTINE PROGRAM LISTING

Note that line 18 takes 10 and not 7 instructions since it is executed when the BC register pair is not zero. In the last pass of the loop however, BC has reached zero, so line 18 is not executed. The clock cycles are therefore:-

Line 15		6 clock cycles
" 16		4 " "
" 17		4 " "
" 18	(not executed)	7 " "
" 19		10 " "
	TOTAL	31 clock cycles

The execution time of the last pass is therefore 31 Tc ns.

If N is the value of the parameter passed to DELAY, then N-1 loops are executed when the parameter is not zero and 1 last pass, when it reaches zero. The total execution time, TD(N), as a function of N is therefore given by:-

$$TD(N) = [24(N - 1) + 31]Tc \text{ ns}$$
$$= (24N + 7)Tc \text{ ns}.$$

1. Rx routine

Refer to Fig E2 where selected portions of the Rx routine program listing are given.

Lines 55 to 57 are a software debounce. The clock cycles are:-

Line 55		10	clock cycles	
" 56		18	" "	
DELAY routine = ((24 X 372) + 7) =		8935	" "	(Note 1)
" 57		4	" "	
	TOTAL	8967	clock cycles	

Note 1: N = DEBNC1 = 174 hexadecimal = 372 decimal.

The execution time of this debounce is therefore:-

$$Ta = 8967 \times Tc$$
$$= 8967 \times 325.521 \text{ ns}$$
$$= 2.919 \text{ ms.}$$

ie Ta is 3 ms approximately.

Lines 64 to 74 are a half bit time delay. The clock cycles are:-

Line 64		10	clock cycles	
" 65		18	" "	
DELAY routine = ((24 X 104) + 7) =		2503	" "	(Note 2)
" 66 to 74	9 X 4 =	36		
	TOTAL	2567	clock cycles	

Note 2: N = DLYHLF = 68 hexadecimal = 104 decimal.

The execution time of this half bit time delay is therefore:-

$$Tb = 2567 \times Tc$$
$$= 2567 \times 325.521 \text{ ns}$$
$$= 0.835 \text{ ms}$$

(= half of 1.67 ms ie half a bit time at 600 Baud)

```
  9 DLYHLF   EQU        68H            ;HALF BIT DELAY FACTOR
 10 DLYA     EQU        0CFH           ;1 BIT DELAY FACTOR

 13 DEBNC1   EQU        174H           ;DEBOUNCE DELAY (1)
 14 DEBNC2   EQU        1300H          ;DEBOUNCE DELAY (2)

 55          LXI  (10)  B,DEBNC1       ;3 MILLISECOND DEBOUNCE
 56          CALL (18)  DELAY          Ta
 57          RIM  ( 4)                 ;IS SID STILL HIGH?
 58          RAL
 59          JNC        ABORT          ;IF NOT, THEN GLITCH RECEIVED

 61 WAIT:    RIM                       ;WAIT FOR START BIT
 62          RLC                       ;HERE YET?
 63          JC         WAIT           ;NO, KEEP WAITING

 64          LXI  (10)  B,DLYHLF       ;HALF BIT TIME DELAY LOOP
 65          CALL (18)  DELAY
 66          NOP  ( 4)                 ;DELAY TRIMMING
 67          NOP  ( 4)
 68          NOP  ( 4)                 Tb
 69          NOP  ( 4)
 70          NOP  ( 4)
 71          NOP  ( 4)
 72          NOP  ( 4)
 73          NOP  ( 4)
 74          RIM  ( 4)                 ;IS START BIT STILL LOW?
 75          NOP  ( 4)                 ;DELAY TRIMMING
 76          NOP  ( 4)
 77          NOP  ( 4)
 78          NOP  ( 4)
 79          NOP  ( 4)
 80          NOP  ( 4)
 81          NOP  ( 4)
 82          NOP  ( 4)
 83          NOP  ( 4)
 84          NOP  ( 4)
 85          NOP  ( 4)
 86          NOP  ( 4)
 87          NOP  ( 4)                 Td
 88          NOP  ( 4)
 89          NOP  ( 4)
 90          NOP  ( 4)
 91          RLC  ( 4)
 92          JC (7/10)  ABORT          ;TERMINATE INT ROUTINE IF NOT
 93 DBMES:   MVI  (10)  M,00H          ;SET START BYTE = 0
 94          INX  ( 6)  H              ;POINT TO NEXT BYTE IN BYTE BUFFER
 95          MVI  ( 7)  A,22D          ;INITIALISE BYTE COUNT
 96 NXTBIT:  STA  (13)  COUNT
 97          LXI  (10)  B,DLYA         ;1 BIT TIME DELAY LOOP
 98          CALL (18)  DELAY
 99          RIM  ( 4)                 ;READ INPUT
100          NOP  ( 4)                 ;DELAY TRIMMING
101          NOP  ( 4)
102          NOP  ( 4)
103          NOP  ( 4)
104          NOP  ( 4)
105          NOP  ( 4)
106          NOP  ( 4)
107          NOP  ( 4)
108          NOP  ( 4)
109          NOP  ( 4)
110          NOP  ( 4)                 Te
111          NOP  ( 4)
112          NOP  ( 4)
113          NOP  ( 4)
114          MOV  ( 7)  M,A            ;STORE INPUT IN BYTE BUFFER
115          INX  ( 6)  H              ;POINT TO NEXT POSITION IN BYTE BUFFER
116          LDA  (13)  COUNT          ;DECREMENT BIT COUNT
117          DCR  ( 4)  A
118          JNZ(7/10)  NXTBIT         ;GOT ALL BITS? IF NOT, READ NEXT BIT

194 ABORT:

203 HI:      RIM                       ;WAIT FOR SID TO GO LOW AGAIN
204          RLC
205          JC         HI
206          LXI  (10)  B,DEBNC2       ;40 MILLISECOND DEBOUNCE
207          CALL (18)  DELAY          Tf
```

FIG E2: RX ROUTINE SOFTWARE TIMING

Lines 75 to 99 are a full bit time delay. The clock cycles are:-

Line 75 to 91	17 X 4	68	clock cycles	
" 92 (not executed)		7	"	"
" 93		10	"	"
" 94		6	"	"
" 95		7	"	"
" 96		13	"	"
" 97		10	"	"
" 98		18	"	"
DELAY routine = ((24 X 207) + 7)	=	4975	"	" (Note 3)
" 99		4	"	"
TOTAL		5118	clock cycles	

Note 3: N = DLYA = CF hexadecimal = 207 decimal.

The execution time of this full bit time delay is therefore:-

Td = 5118 X Tc
= 5118 X 325.521 ns
= 1.666 ms
(= a bit time at 600 Baud)

Lines 100 to 118, then back to 96 and then to 99 are a full bit time delay loop. The clock cycles are:-

Line 100 to 113	14 X 4	56	clock cycles	
" 114		7	"	"
" 115		6	"	"
" 116		13	"	"
" 117		4	"	"
" 118 (executed)		10	"	"
" 96		13	"	"
" 97		10	"	"
" 98		18	"	"
DELAY routine = ((24 X 207) + 7)	=	4975	"	" (Note 3)
" 99		4	"	"
TOTAL		5116	clock cycles	

The execution time of this full bit time delay loop is therefore:-

Te = 5116 X Tc
= 5116 X 325.521 ns
= 1.665 ms
(= a bit time at 600 Baud)

Lines 206 and 207 are a software debounce. The clock cycles are:-

Line 206	10 clock cycles	
" 207	18 " "	
DELAY routine = ((24 X 4864) + 7) =	116743 " "	(Note 4)
TOTAL	116771 clock cycles	

Note 4: N = DEBNC2 = 1300 hexadecimal = 4864 decimal.

The execution time of this debounce is therefore:-

Tf = 116771 X Tc
= 116771 X 325.521 ns
= 38.011 ms.

ie Tf is 40 ms approximately.

The following should be related to the discussion in Appendix C:-

(i) Ta is the debounce period used to avoid jitter on the RXD output of the modem when the Rx routine is entered.

(ii) Tb is the half bit time delay used to synchronise the input data strobing to the centre of the start bit.

(iii) Td is the full bit time delay used to clock in the first data bit after the start bit.

(iv) Te is the full bit time delay loop which is used to clock in the subsequent 21 bits.

(v) Tf is the debounce period used to avoid the jitter on the RXD output of the modem caused by the burst of white noise from the outstation u.h.f. radio receiver squelch.

Note that the two debounce periods Ta and Tf are not critical as long as they are of sufficient duration to avoid the RXD output jitter in each case.

However, periods Tb, Td and Te are critical since they affect the data input strobing at the CPU SID line which must be at exactly 600 Baud. In these cases, the parameter N passed to the DELAY routine is the coarse control and the NOP instructions provide the fine tuning needed to trim these periods exactly.

Notice the overlapping of lines 96 to 99 in the periods Td and Te. Once Td has been trimmed then Te can subsequently be fine tuned.

Poll loop WAIT (lines 61 to 63) defines the start bit edge synchronisation to which all subsequent input data strobing is referenced. Poll loop HI (lines 203 to 205) detects the end of the VFT signal after the stop bit (in the absence of a VFT signal the SID line of the CPU is low).

With reference to Fig 1.3 the Rx routine timing may be summed up as follows:-

(i) When there is no VFT signal, the SID line of the CPU is low.

(ii) When the pretone is received it generates an RST 6.5 interrupt and the SID line goes high; the Rx routine is entered.

(iii) After debounce period Ta, the SID line is checked to confirm that it is still high; if not the Rx routine is aborted.

(iv) Poll loop WAIT waits for the negative going start bit edge at the SID line; when it arrives, synchronisation has been achieved.

(v) After half bit period Tb, the middle of the start bit is sampled and it is checked to confirm that it is low; if not, the Rx routine is aborted.

(vi) After full bit period Td, the first data bit of the message is clocked in.

(vii) The remaining 21 bits of the message are clocked in using 21 passes of the period Te.

(viii) After the stop bit has been clocked in, POLL loop HI waits for the VFT signal to cease.

(ix) After debounce period Tf the Rx routine is exitted.

Steps (i) to (ix) demonstrate a very tightly controlled timing sequence which is necessary for successful reception of a message.

This describes all the Rx routine timing.

2. Tx routine data output strobing

Refer to Fig E3 where a portion of the Tx routine program listing is given.

Lines 42 to 52, then back to 38 and then to 41 are a full bit time delay. The clock cycles are:-

Line	42		13 clock cycles	
"	43		4 " "	
"	44		13 " "	
"	45	(not executed)	7 " "	
"	46		6 " "	
"	47		10 " "	
"	48		18 " "	
DELAY routine		= ((24 X 208) + 7) =	4999 " "	(Note 5)
"	49 to 51	3 X 4 =	12 " "	
"	52		10 " "	
"	38 to 40	3 X 7 =	21 " "	
"	41		4 " "	
		TOTAL	5117 clock cycles	

Note 5: N = DLY = D0 hexadecimal = 208 decimal.

The execution time of this full bit time delay is therefore:-

$$
\begin{aligned}
Tg &= 5117 \times Tc \\
&= 5117 \times 325.521 \text{ ns} \\
&= 1.666 \text{ ms} \\
&\text{(= a bit time at 600 Baud)}
\end{aligned}
$$

Note that the Tx routine timing is very straight forward compared with the Rx routine timing since it merely strobes the data out to the SOD line of the CPU to the TXD input of the modem at 600 Baud.

```
 7 DLY      EQU        0D0H          ;1 BIT DELAY FACTOR


38 NXTBIT: MOV ( 7)   A,M           ;GET BYTE
39         ORI ( 7)   01000000B     ;MAKE SURE SDE=1
40         ANI ( 7)   11100111B     ;MAKE SURE MSE=0
41         SIM ( 4)                 ;OUTPUT MS BIT
42         LDA (13)   COUNT         ;DECREMENT BIT COUNT
43         DCR ( 4)   A
44         STA (13)   COUNT
45         JZ(7/10)   NEXT          ;JUMP OUT IF MESSAGE FINISHED
46         INX ( 6)   H             ;INCREMENT BYTE POINTER
47         LXI (10)   B,DLY         ;WAIT 1 BIT TIME
48         CALL(18)   DELAY
49         NOP ( 4)                 ;DELAY TRIMMING
50         NOP ( 4)
51         NOP ( 4)
52         JMP (10)   NXTBIT        ;OUTPUT NEXT BIT
53 NEXT:
```

Tg

FIG E3: TX ROUTINE OUTPUT DATA STROBING

APPENDIX F

1 SECOND INTERRUPT ROUTINE (SEC)

Refer to the simplified flow chart of Fig F1. This routine is initiated by a once-a-second clock pulse from the PWT module on the RST 7.5 interrupt input of the CPU (refer paragraph 3.3(ii)). Notice that unlike the Rx and Tx interrupt routines, the 1 Second interrupt routine is latched, so if it cannot be serviced immediately, it will not be lost (refer paragraph 3.7.1.1(iii)). For further details of the latched nature of the RST 7.5 interrupt, the reader should consult the 8085 manual.

On entering the 1 Second routine, the SECBUSY flag (refer paragraph 4.4) is set; as explained in the Rx and Tx routines, this flag controls the exit path of these routines (refer paragraph 4.3(i)). The '1SEC' LED is toggled and the 'B/GRND' LED is switched off. The Rx and Tx routines are re-enabled since they have higher priority (refer paragraph 4.3). The alternate second flag, ALTSEC (refer paragraph 4.4) is polled and if set, execution of the rest of SEC proceeds, otherwise most of the routine is bypassed.

The logic which follows now, concerning the selection of either positive or negative A/D module values, is identical to when the initial memory image was established in the INIT routine as explained in Appendix J. The essential difference here is that only one analogue channel is sampled every alternate second ie once every two seconds, whereas in the INIT routine, all the channels are sampled and stored.

The reason for alternate second sampling is as follows:-

It takes exactly one second to perform an A/D conversion as explained in Appendix G, but because of its lower priority, if an Rx or Tx routine is being executed when a 1 Second interrupt occurs, then it is not serviced until the end of that routine and so the initialisation of an A/D conversion could be delayed somewhat; worst case would be when the 1 Second interrupt occurs at the beginning of an Rx interrupt routine when a double message request

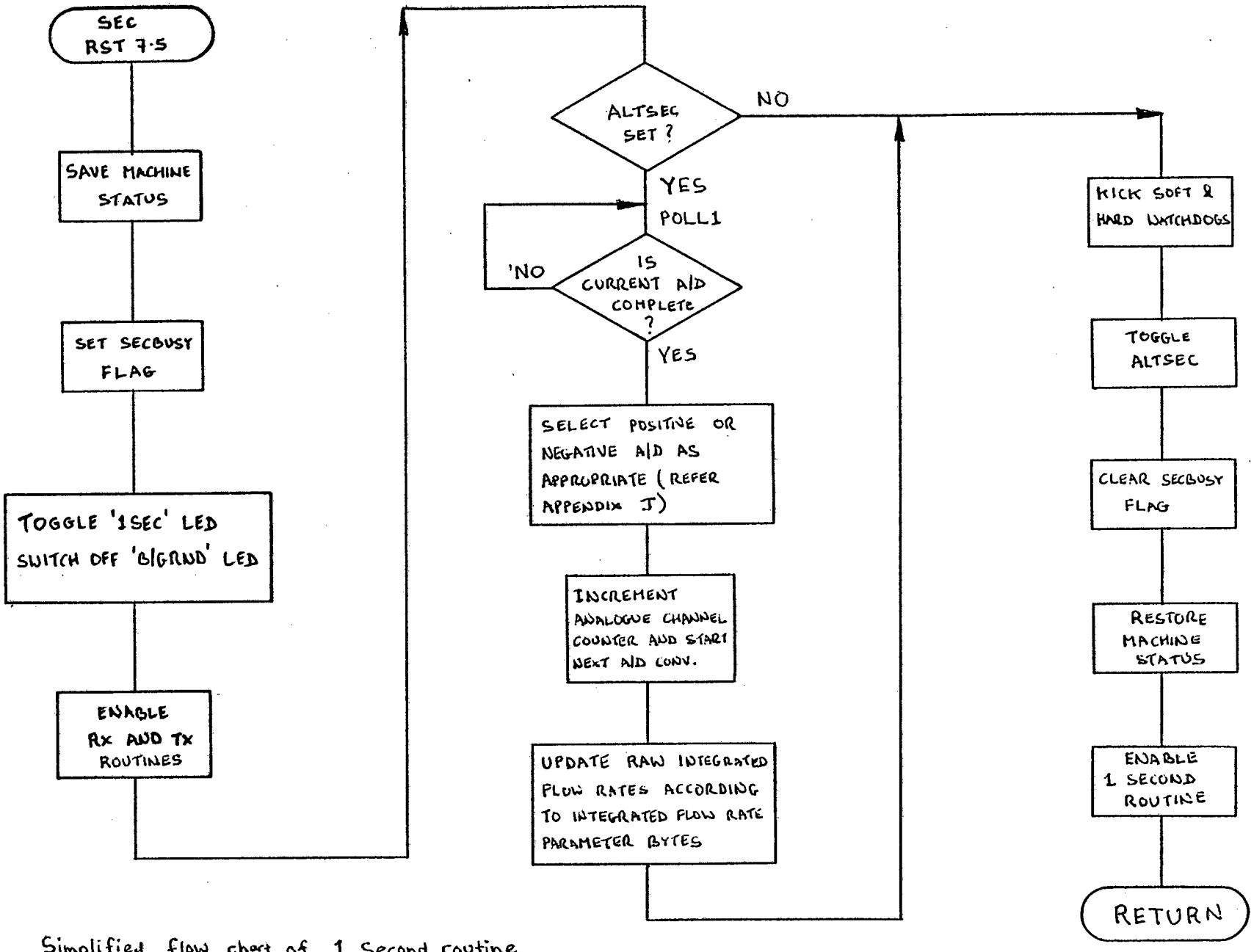


Fig F1 Simplified flow chart of 1 Second routine

word is being received from the master station (ie 93 ms as shown in Fig 1.3 and explained in paragraph 1.5.2(v)). The identical polling of the MS bit of the control register of the PIT on the A/D is used, as is explained in Appendix G, so this would mean that since the 1 Second routine has been delayed by 93 ms then the poll loop would run for 93 ms ie almost a tenth of a second. This would be an unnecessary waste of processor time, so if alternate second A/D conversion is done, then the conversion is guarenteed to be complete by the time the poll loop is encountered.

Each time an A/D conversion is completed, the raw value analogue storage pointer and the channel counter are incremented and if all ten channels have been sampled, the analogue storage pointer is re-initialised back to the beginning of the raw analogue level buffer RAWALV (refer paragraph 4.4) and the channel counter is wrapped around to select the first analogue channel for the next conversion. The positive and negative A/D counters are then re-initialised, the current analogue channel selected and both positive and negative conversions initiated together as explained in Appendix J.

The next logical block deals with the calculation of the raw integrated flow rates. Associated with each integrated flow rate is an integrated flow rate parameter byte; there are up to three integrated flow rates in the outstation, each one of which can be the average of any selection of 1 to 8 of the flow rates (refer paragraph 3.2). This selection of the flow rates is determined by which bits in the parameter byte of the integrated flow rate in question are set; these bits are read from switch banks B, C and D of the PWT board for integrated flow rates 1 to 3 respectively. For example, if integrated flow rate 2 is the average of the integrals of flow rates 2, 3, 6 and 8 then switches 2, 3, 6 and 8 on switch bank C of the PWT board must be ON (refer paragraph 3.7.2.1). The software adds together the flow rates 2, 3, 6 and 8 to the partial sum and counts the number of bits in the parameter bug (in this case four) and writes this to the divisor buffer for the integrated flow rate in question (refer paragraph 4.4). This divisor is used by the Background Task in calculating the average of the integrals of the flow rates in question (refer Appendix I).

So in this case:-

$$\text{INTEGRATED FLOW RATE 2} = 1/4\ [\int \text{FLOW RATE 2} + \int \text{FLOW RATE 3} + \int \text{FLOW RATE 6} + \int \text{FLOW RATE 8}]$$

The partial sum for each integrated flow rate is the sum of the time integrals of the flow rates selected by the corresponding parameter byte, from the last integrated flow reset to the present time; this was dicussed in paragraph 2.4.1. This partial sum is therefore monotonically increasing in time and is updated every two seconds. For a fuller treatment of the integrated flow rate philosophy refer to Appendix H. This summation is an on-going process which is usually reset once in 24 hours. This process is done for each of the three integrated flow rates, calculating three partial sums.

What follows on from here happens every second; the watchdog timer one-shots on the PWT and PWR modules are triggered, the alternate second flag ALTSEC is toggled, the SECBUSY flag (refer paragraph 4.4) is cleared since the 1 Second routine is nearly finished, and the 1 Second routine itself is re-enabled.

APPENDIX G

CONTROL OF 8254 PIT'S WITH PRESCALED CLOCK INPUTS

The 8254 PIT consists of three timer modules which may be used in a variety of ways. On the PWT and A/D modules, only the binary modes 0, 1 and 2 are of interest. The reader is referred to the 8254 manual for the other modes.

It is important to note the consequences of cascading two of these counters as shown in Fig G1, where counters A and B are cascaded.

Let the input frequency to counter A at CLKA be f1. If counter A is initialised with a count M and operated in mode 2 ie a divider, the frequency at OUTA is f1/M.

Suppose that counter B has its CLKB input connected to OUTA and is operated in mode 1 ie a retriggerable one shot multivibrator. If it is initialised with a count of N and is triggered at its GATEB input, its output OUTB does not go low until the first pulse arrives at its CLKB input. This behaviour is due to its synchronous nature and has a very significant effect as follows:-

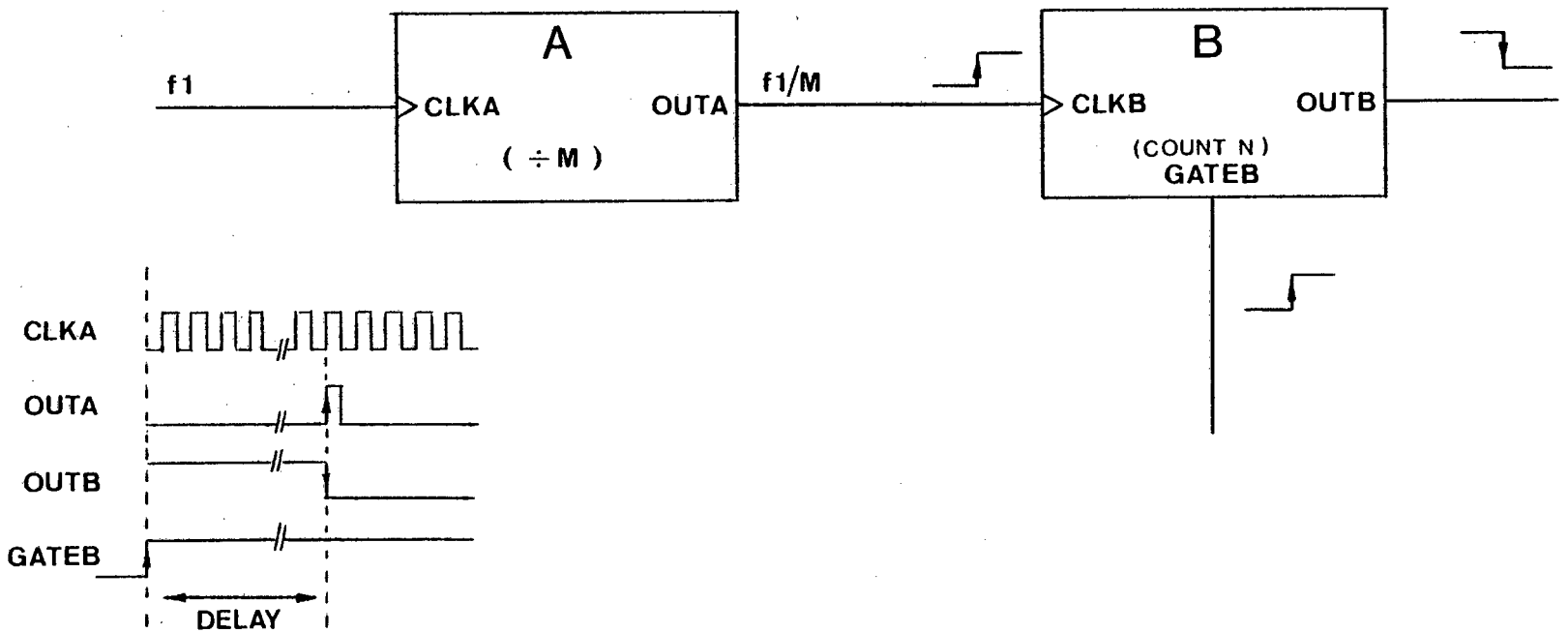
Counter A divides the frequency f1 by M, so up to M cycles can elapse at its input CLKA before a pulse arrives at its output to trigger counter B. The timing diagram on Fig G1 illustrates this. Counter A therefore prescales the f1 signal for counter B and causes this delay of up to M cycles at CLKA between the CLKB trigger and the OUTB response.

In the absence of any further trigger signals at the GATEB input, OUTB stays low for

$$M \times N \text{ clock cycles} = (M \times N)/f1 \text{ seconds.}$$

This is how the A/D converter works, where M and N are chosen so that

$$(M \times N)/f1 = 1 \text{ second.}$$



CASCADED COUNTERS | Fig G1

This 1 second period is used to gate pulses through to a third counter.

If, however, counter B is triggered before it has expired, then this output remains low and will continue to do so provided it is triggered often enough. This is how the PWT soft watchdog works where

$$(M \times N)/f1 = 1.5 \text{ seconds approximately}$$

and counter B is triggered every second from a third counter.

The status of OUTB can be determined by polling the MS bit of the control register of counter B; when it is 1, OUTB is high and vise versa. The software safe-guards which follow are based on this.

For both the A/D and PWT modules,

$$f1 = 3.072 \text{ MHz}$$

from the SABUS system clock. M and N are chosen as described below.

1. PWT module initialisation

Fig G2 is made up of selected portions of the program listing of the Initialisation routine. Lines 148 to 165 load counters 0, 1 and 2 of the 8254 PIT. On the PWT module counter 0 is the prescaler for counters 1 and 2.

Counter 1 generates the 1 Second interrupt. For this pair, therefore

M = FF7D hexadecimal = 65405 decimal (lines 150 and 152)
and N = 2F hexadecimal = 47 decimal (lines 156 and 158).

Therefore,

(M X N)/f1 = (65405 X 47)/3.072 MHz = 1.000662435 seconds.

During in-circuit emulation, M and N were trimmed to get as close as possible to 1 second exactly.

Counter 2 is the soft watchdog and is initialised to give a time-out period of approximately 1.5 seconds (lines 160 to 165). This is not at all critical, as long as it is greater than 1 second since it is triggered by counter 1 every second.

Refer paragraph 3.7.1.2(iv) for further details.

On line 166, counter 2 is triggered by an output-write instruction. As explained above, it does not respond immediately since its input is prescaled. Therefore, the poll loop POLL (lines 167 to 171) is executed where the MS bit of counter 2's control register is interrogated. As soon as this bit goes low, the program jumps out of the poll loop.

Lines 172 and 173 initialise the 8255A as described in Appendix J and since counter 2 has gone low, it is safe to enable its output through to the $\overline{\text{RESET IN}}$ line of the SABUS by bit 2 of the C port of the 8255A.

Refer to Fig 3.4 for the interconnection of the three counters and the enabling of the soft watchdog timer.

```
148             MVI     A,00110100B     ;SELECT COUNTER 0 DOUBLE BYTE
149             OUT     LOW PCNTWD      ;MODE 2 BINARY CONTROL BYTE
150             MVI     A,7DH           ;LOAD COUNTER 0 WITH FINE COUNT
151             OUT     LOW PCNTR0
152             MVI     A,0FFH
153             OUT     LOW PCNTR0
154             MVI     A,01110100B     ;SELECT COUNTER 1 DOUBLE BYTE
155             OUT     LOW PCNTWD      ;MODE 2 BINARY CONTROL BYTE
156             MVI     A,2FH           ;LOAD COUNTER 1 WITH COARSE COUNT
157             OUT     LOW PCNTR1      ;FINE X COARSE +/- 1500 MILLISECONDS
158             MVI     A,0
159             OUT     LOW PCNTR1
160             MVI     A,10110010B     ;SELECT COUNTER 2 DOUBLE BYTE
161             OUT     LOW PCNTWD      ;MODE 1 BINARY CONTROL BYTE
162             MVI     A,150D          ;LOAD COUNTER 2 WITH +/- 1.5 SEC
163             OUT     LOW PCNTR2      ;1-SHOT TIME
164             MVI     A,0
165             OUT     LOW PCNTR2
166             OUT     LOW ONESHT      ;KICK COUNTER 2 AND POWER MODULE
                                        ;AND POWER MODULE 1-SHOT
167 POLL:       MVI     A,11101000B     ;POLL ONE-SHOT STATUS
168             OUT     LOW PCNTWD
169             IN      LOW PCNTR2
170             RAL
171             JC      POLL
172             MVI     A,90H           ;INITIALISE 8255A WHEN ONE-SHOT
                                        ;O/P GOES LOW
173             OUT     LOW PWT         ;A-PORT I/P, B-PORT O/P, C-PORT O/P


176             MVI     A,00000000B     ;SELECT LS PARAMETER BUG ('PORT A')
177             OUT     LOW PRTSEL      ;AND ENABLE 8254 SYSTEM RESET ONE-SHOT
```

FIG G2: PWT MODULE INITIALISATION

2. Establishment of initial memory image

Fig G3 is made up of selected portions of the program listing of the Initialisation routine. Lines 83 to 100 load counters 0, 1 and 2 of the 8254 PIT. On the A/D module counter 2 is the prescaler for counters 0 and 1. Counter 1 is used to generate a 1 second window which is used to gate pulses from the voltage-to-frequency converter through to counter 0.

For counter 2,

M = FF5F hexadecimal = 65375 decimal (lines 97 and 99)

and for counter 1,

N = 2F hexadecimal = 47 decimal (lines 91 and 93).

Therefore

(M X N)/f1 = (65375 X 47)/3.072 MHz = 1.000203451 seconds.

which is very close to 1 second; this was trimmed while testing the software on the in-circuit emulator.

Refer paragraph 3.8.1.2(iii) for further details.

The negative A/D board is initialised identically but is not shown here.

The initial memory image must now be established as follows:-

Line 204 initialises the raw analogue value pointer to RAWALV, described in paragraph 4.4. Line 205 initialises the channel counter. Line 206 triggers the soft and hard watchdog timers. The reason for this is about to become apparent. Lines 207 to 211 initialise both positive and negative A/D board counters (where applicable). Lines 212 to 214 select the current analogue input channel via the analogue multiplexer on the A/D module and start an A/D conversion. A two stage polling sequence then follows:-

POLL1 is a poll loop (lines 215 to 219) which waits for counter 1 to respond. When it has responded, POLL2 is entered (lines 220 to 224) which waits for counter 1 to time-out. Because counter 1 is programmed for the one-second window period mentioned above,

```
204             LXI     H,RAWALV        ;POINT TO START OF
                                        ;RAW ANALOGUE VALUE TABLE
205             MVI     C,0             ;INITIALISE CHANNEL COUNTER
206 NXTVAL:     OUT     LOW ONESHT      ;KICK WATCHDOG TIMERS ON PWT
                                        ;AND POWER MODULES
207             MVI     A,0FFH          ;INITIALISE ANALOGUE CONVERSION COUNTER
208             OUT     LOW ACTR0P      ;POSITIVE A/D BOARD
209             OUT     LOW ACTR0P
210             OUT     LOW ACTR0N      ;NEGATIVE A/D BOARD (REGARDLESS)
211             OUT     LOW ACTR0N
212             MOV     A,C             ;SELECT CURRENT CHANNEL
213             OUT     LOW CHNSEL
214             OUT     LOW STRCNV      ;START CONVERSION
215 POLL1:      MVI     A,11100100B     ;WAIT FOR 1 SHOT TO GO LOW
216             OUT     LOW ACNWDP      ;DUE TO SLOW PRE-SCALED CLOCK
217             IN      LOW ACTR1P      ;AND NULL COUNTS
218             RAL
219             JC      POLL1           ;IF STILL HIGH THEN WAIT
220 POLL2:      MVI     A,11100100B     ;IS CONVERSION COMPLETE?
221             OUT     LOW ACNWDP      ;IE GET STATUS OF COUNTERS 1 & 0
222             IN      LOW ACTR1P      ;HAS CONVERSION TIME ELAPSED (1 SHOT)?
223             RAL
224             JNC     POLL2           ;WAIT UNTIL CONVERSION COMPLETE


266 STORE:      MOV     M,E             ;STORE DATA IN RAW ANALOGUE VALUE LIST
267             INX     H
268             MOV     M,D
269             INX     H
270             INR     C               ;ALL CHANNELS SAMPLED?
271             MOV     A,C
272             CPI     LOW CHNUM
273             JNZ     NXTVAL          ;NO, SAMPLE NEXT CHANNEL
```

FIG G3: A/D MODULE CONTROL FOR ESTABLISHMENT OF INITIAL MEMORY IMAGE

POLL2 is of exactly one second's duration. This means that it takes exactly one second to do an A/D conversion; for this reason it is necessary to trigger the soft watchdog prior to an A/D conversion otherwise it would time-out (the soft watchdog timer on the PWT module has an expiry time of approximately 1.5 sec as mentioned in paragraph G1), causing an unwanted system restart.

The converted value gets transferred to the DE register pair and stored in memory at the current address in the raw analogue value pointer (lines 266 to 269). Lines 270 to 273 increment the channel counter and the program returns to NXTVAL to convert the next analogue value.

This loop continues until all analogue channels have been converted whereupon the initial memory image is now established.

Refer to Fig 3.5 for the interconnection of the three counters.

3. A/D conversions controlled by 1 Second routine

Fig G4 is a short extract from the program listing of the 1 Second routine.

Lines 66 to 70 are a polling loop which polls the MS bit of the control register of counter 1; only when it has timed out ie the A/D conversion is complete, will the program jump out of the poll loop. Since alternate second sampling is done, as explained in Appendix F, the need for this polling is largely obviated since the A/D conversion is gaurenteed to be complete by this time; however it was included for completeness.

```
66 POLL1:   MVI     A,11100100B     ;IS CONVERSION COMPLETE?
67          OUT     LOW ACNWDP
68          IN      LOW ACTR1P
69          RAL
70          JNC     POLL1           ;WAIT UNTIL CONVERSION COMPLETE
```

FIG G4: A/D MODULE CONTROL IN 1 SECOND ROUTINE

APPENDIX H

INTEGRATED FLOW RATE ARITHMETIC PROCESSING

The A/D module has a range of from 0 to 10 000. Thus the maximum converted value for each flow rate is 10 000. As explained in the SEC module (Appendix F), each raw total is calculated as the summation of a selection of up to eight flow rates, so the maximum value attainable for a raw total is 80 000 ie when all eight flow rates are selected and all are at the maximum value all the time.

This numerical integration is done every alternate second so the maximum accumulated partial sum is:-

$$24 \times 60 \times 60 \times 0.5 \times 80\,000 = 3\,456\,000\,000 \text{ decimal}$$
$$= \text{CD FE 60 00 hexadecimal}$$

so four bytes are needed to accumulate the partial sum hence four bytes per partial sum in the SEC module.

The Background Task then takes this value and multiplies it by the binary fraction as selected by the divisor pointer calculated in SEC (refer to Appendices F and I); this result is then the required average raw integrated flow rate and has a maximum value of:-

$$3\,456\,000\,000 / 8 = 432\,000\,000 \text{ decimal}$$
$$= \text{19 BF CC 00 hexadecimal.}$$

This 4-byte raw value ranging from 0 to 432 000 000 decimal must result in a printout range of 0 to 999 999 ML (refer Appendix A) so the raw total must be scaled by the 24-hour normalising factor 1/432; the result is then converted to BCD to give the final integrated flow rate ready for reply words. This processing is done in the Background Task (refer Appendix I).

The divisors and the normalising factor are represented as 31-bit binary fractions to give maximum accuracy in the multiplication process ie MULT multiplies a 32-bit (ie 4-byte) integer by a 31-bit binary fraction producing a 32-bit result. The binary fraction is 31-bits and not 32-bits because the MULT routine uses a successive shift/add technique of the integer (refer paragraph 4.5.14) and after 32 shifts the integer would be zero and hence the least significant bit of the binary fraction would be ineffective.

APPENDIX I

BACKGROUND TASK (BACK)

Refer to the simplified flow chart in Fig I1. This routine runs whenever no Rx, Tx or 1 Second interrupt routine is running; at the end it loops back to the beginning and does so continuously (except for when the Initialisation routine is in progress (refer Appendix J). At the beginning of the routine, the 'B/GRND' LED is switched on and the BCD buffer control flag CNTRL is polled (refer paragraph 4.4); if it is clear then it is set and an offset word is set to zero; if CNTRL is set it is cleared and the offset word is preset to a value equal to the offset between LVLBASE and DBUFF (refer paragraph 4.4). This offset word is used to control access to the BCD buffers; if it is zero then the BCD buffer starting at LVLBASE is accessed; if it is preset then the mirror buffer DBUFF is accessed. Thus on each pass of the Background Task, CNTRL is toggled so access to the two BCD buffers is alternated; the reason for this is explained in paragraph 4.4 where DBUFF is described.

The two raw analogue levels are then converted to BCD and packed into LVLBASE as in Fig 4.3(a). Next, the eight raw flow rates are converted to BCD and packed into FLBASE as in Fig 4.3(b). The routine BCD is used to do this.

The next section is a little more complex. For each of the three integrated flow rates in the outstation, the corresponding number in the divisor buffer (calculated in the 1 Second routine) is used to select a binary fraction from a look-up table; this fraction is the reciprocal of the number of bits set in the parameter byte as read from the switch bank on the PWT board, for the integrated flow rate in question (this is explained in Appendix F). For the trivial cases of 0 or 1 bits set, the fraction is set to 0 or 1 respectively. The partial sum for the integrated flow rate (refer to Appendix F) is then multiplied by the selected fraction and then again by the 24-hour normalising factor (explained in Appendix H). This result is then finally converted to BCD and packed into IFBASE as in Fig 4.3(c). This process is done for all three integrated flow rates and was mentioned in paragraph 2.4.2.4.

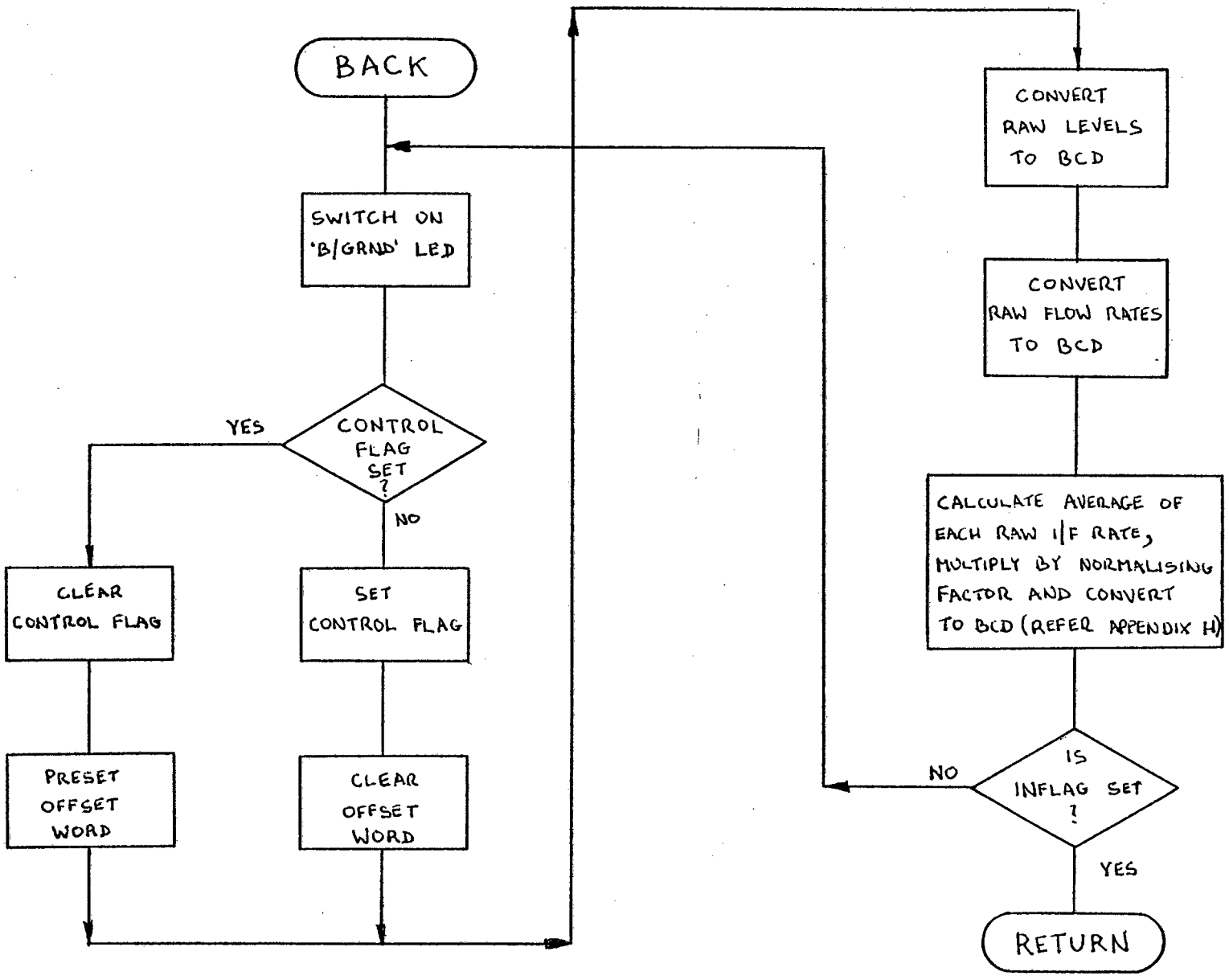


Fig I 1 Simplified flow chart of Background Task

The 'Initialisation in progresss' flag INFLAG is polled; the significance of this flag is explained in paragraph 4.4. If INFLAG is not set then BACK loops back to the beginning; if set then BACK is treated by INIT as a subroutine - this only happens during initialisation.

APPENDIX J

INITIALISATION ROUTINE (INIT)

All the hardware on the SBC, PWT, A/D and MODEM hardware modules is initialised.

The SBC has an 8255A PPI (Programmable Peripheral Interface) which is initialised as all three ports as outputs; the RTS line from the SBC to the modem is bit 0 of the A port and is set high since this is a negative edge triggered input; the SOD line of the CPU is set to 1 so that when the outstation replies, the start bit = 0 will cause the necessary change of state for start bit synchronisation at the master station (refer to Fig 4.4); the 1K of user RAM on the SBC is cleared.

The A/D board has an 8254 PIT (Programmable Interval Timer). Counter 2 is used as a prescaler for counter 1 which is used as a one-shot with a window time of exactly one second; this is used to gate the voltage-to-frequency converter pulses through to counter 0 which holds the converted analogue value; two A/D boards are initialised, one for positive analogue input values and the other for negative values (if required). Refer paragraph 3.8.1.2(iii).

The 'Initialisation in progress' flag, INFLAG, is set for use by Background Task later on during initialisation (refer paragraph 4.4).

The PWT module has an 8254 PIT and an 8255A PPI which are initialised as follows:-

The 8254 PIT uses counter 0 as a prescaler for counters 1 and 2. Counter 1 is initialised with a value such that the product of counter 0 and counter 1 divider ratios divides the system clock frequency down to exactly 1 Hz; this is used as the 1 Second interrupt which initiates the 1 Second routine.

Counter 2 is initialised with a value such that it forms a re-triggerable one shot with an expiry time of approximately 1.5 seconds; this is the primary watchdog timer for the outstation and is retriggered once a second by the 1 Second routine, so a generous 50% margin is allowed. Refer paragraph 3.7.1.2(iv). There is also an analogue watchdog timer on the PWR module with a much longer time-out period which is triggered simultaneously with the primary watchdog timer on the PWT module; refer paragraph 3.7.2.3 for further details.

The soft watchdog watchdog timer is then triggered and when it has responded, the 8255A is initialised as follows:-

The A port of the 8255A is initialised as an input port which is used to read four mutiplexed 8-bit switch banks, ie switch banks A, B, C and D. The B port is initialised as outputs to drive eight status indicator LED's displaying outstation status. The C port is initialised as an output port where bits 0 and 1 are used to multiplex the four switch banks to the A port inputs and bit 2 is used to enable the soft watchdog timer (see below). Refer paragraph 3.7.1.2 (ii) and (iii).

Note that only when the watchdog timer has responded ie its output gone low will its output be enabled through to the $\overline{\text{RESET IN}}$ line of the SABUS by bit 2 of the C port of the 8255A.

Refer to Appendix G for a full description of the PWT module initialisation.

A bit on the B port is used to switch on the 'RESTART' LED. This completes the initialisation of the PWT module.

The MODEM module has an 8254 PIT where the three timers are used to generate the necessary timing for the modem and u.h.f. radio control as explained in paragraph 2.2. Recall paragraph 1.5.3 and Fig 1.3 where the necessary request word/reply word protocol was described. The timing diagram on the circuit diagram of the modem, Fig 3.3 illustrates how these timing parameters are achieved by initialising the counters of the 8254 PIT with the appropriate values.

An initial memory image comprising all analogue input values is established before the outstation is allowed to reply; this is to prevent zero values from being sent back to the master station after outstation initialisation. This could easily happen if the initial memory image were not established because the 1 Second routine updates only one analogue value every two seconds (this is discussed in Appendix F).

A similar precaution which is exercised for the initialisation of the soft watchdog timer on the PWT module is also necessary at this point; refer to Appendix G for details concerning the A/D module initialisation and usage.

When both positive and negative analogue values relative to analogue common are to be scanned, then an additional negative A/D board must be installed. Recall that all the input signals of an A/D module must be of the same polarity; refer paragraph 3.8.1.1. Those channels which are negative will be connected to the negative A/D board, with the corresponding channels on the positive A/D board unused, so these positive channels will return zero values (or very small, a value of 10 counts over a range of 0 to 10 000 is considered small enough) when scanned. When a negative A/D board is installed, switch 7 of switch bank bank A of the PWT board should be configured as a '1' so the software can establish that a negative A/D board is present. Refer paragraph 3.7.2.1.

Refer now to Fig J1 for the logic controlling the positive and negative A/D board selection:-

If the positive analogue value is zero, check if a negative A/D board is installed; if not, then take the zero value as the correct one.

If a negative A/D board is installed, however, then read the negative analogue value and take this as the value. If on first reading the positive value the reading is not zero, but greater than 10, then accept this as the value; if the value is less than 10 then it is possible that no signal is present on the positive A/D board on that channel so check if a negative A/D board is installed as before. This process is done for 10 analogue channels (2 levels and 8 flow rates).

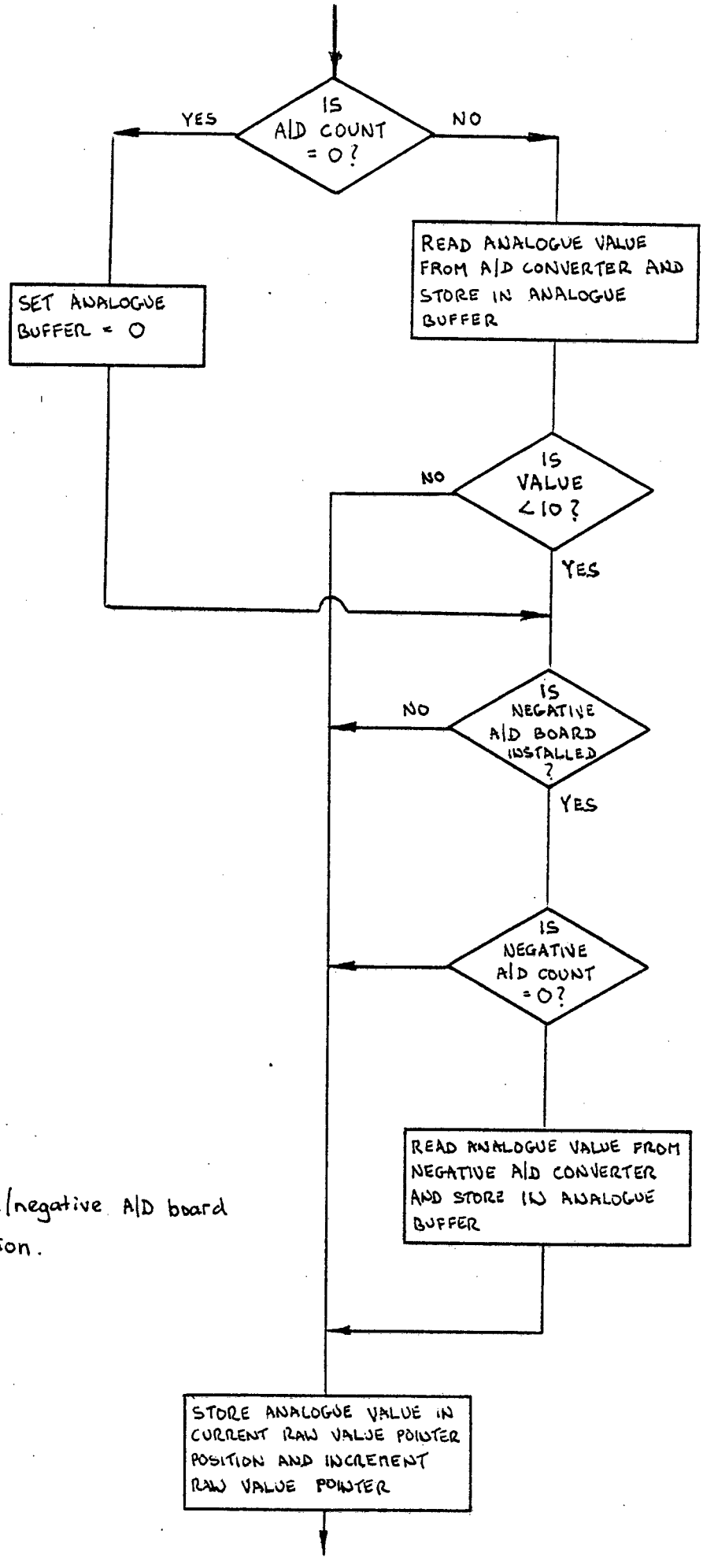


Fig J1 Positive/negative A/D board selection.

This establishes the initial raw level (RAWALV) and raw flow rate (RAWAFL) buffers referred to in paragraph 4.4. Note that when an A/D conversion is initiated, both the positive and negative (if required) A/D one-shots are triggered since both boards are programmed to respond to the same software 'convert' instruction. Since both one-shots run off the same system clock, they are locked together synchronously and both their one-second window periods will expire at precisely the same instant; hence it is only necessary to poll the control register of the positive A/D one-shot to establish when the A/D conversion is complete, as described in Appendix G.

The Background Task is then called twice as a subroutine so that both the LVLBASE, FLBASE and IFBASE buffers and the mirror buffer DBUFF can be established as the initial memory image. Recall that INFLAG has been set earlier on in the Initialisation routine so the Background Task returns to this routine. This is the only time that the Background Task is called as a subroutine; from now on it will run in a loop.

The positive and negative A/D counters are then prepared for another conversion; Analogue Channel 0 is selected and an A/D conversion is initiated; this time, unlike when the initial memory image was being established, the software does not wait for the A/D conversion to be completed - this will be done in the 1 Second routine from now on and is explained fully in Appendix F.

This is the end of the Initialisation routine so the 'RESTART' LED is switched off and INFLAG is cleared. This ensures that the Background Task will run in a loop from now on. The 1 Second and Rx interrupt routines are enabled and the Background Task is entered.

APPENDIX K

DIGITAL INPUT ROUTINE (DIGIN)

Before dealing with the actual routine itself, a closer look at how the point address bits are assigned for digital input request words is necessary; this was briefly mentioned in paragraph 1.5.3. Refer to Fig 1.4.

When bit 8 = 1, then an alarm or level is being requested. Bits 6 and 7 play no part here, but are actually set to zero. Bits 9 to 12 are then used as a 4-bit sub-address; when it is 1, the one and only alarm word is being requested; when it is 2, 3, 4 etc then level digits are being asked for (recall that two request/reply sequences are necessary for levels ..... refer paragraph 1.5.3). These sub-addresses occur in even/odd pairs for each level with the lower sub-address being even and referring to BCD4 of the level and the higher sub-address being odd and referring to BCD's 0 to 3 of the level (refer Fig 1.5).

For example,

sub-address = 2 refers to BCD4 of level 1
sub-address = 3 refers to BCD's 0 to 3 of level 1
sub-address = 4 refers to BCD4 of level 2

and so on.

When bit 8 = 0, then all the other bits 6, 7 and 9 to 12 are also zero, and then either the least or most significant BCD's of an integrated flow rate are being requested; the actual digits requested are determined by the status output double message request word immediately prior to the integrated flow request as mentioned in paragraph 1.5.3(i) to (vi) and explained fully in Appendix L.

Refer now to Fig 4.4 and Fig K1. The DIGIN routine tests bit 8 of the point address; if it is zero then it uses the integrated flow rate digit pointer to access the required integrated flow rate digits and transfer them to the packed message word. The integrated flow rate digit pointer is determined by the STOUT routine from information in the status output double message request word

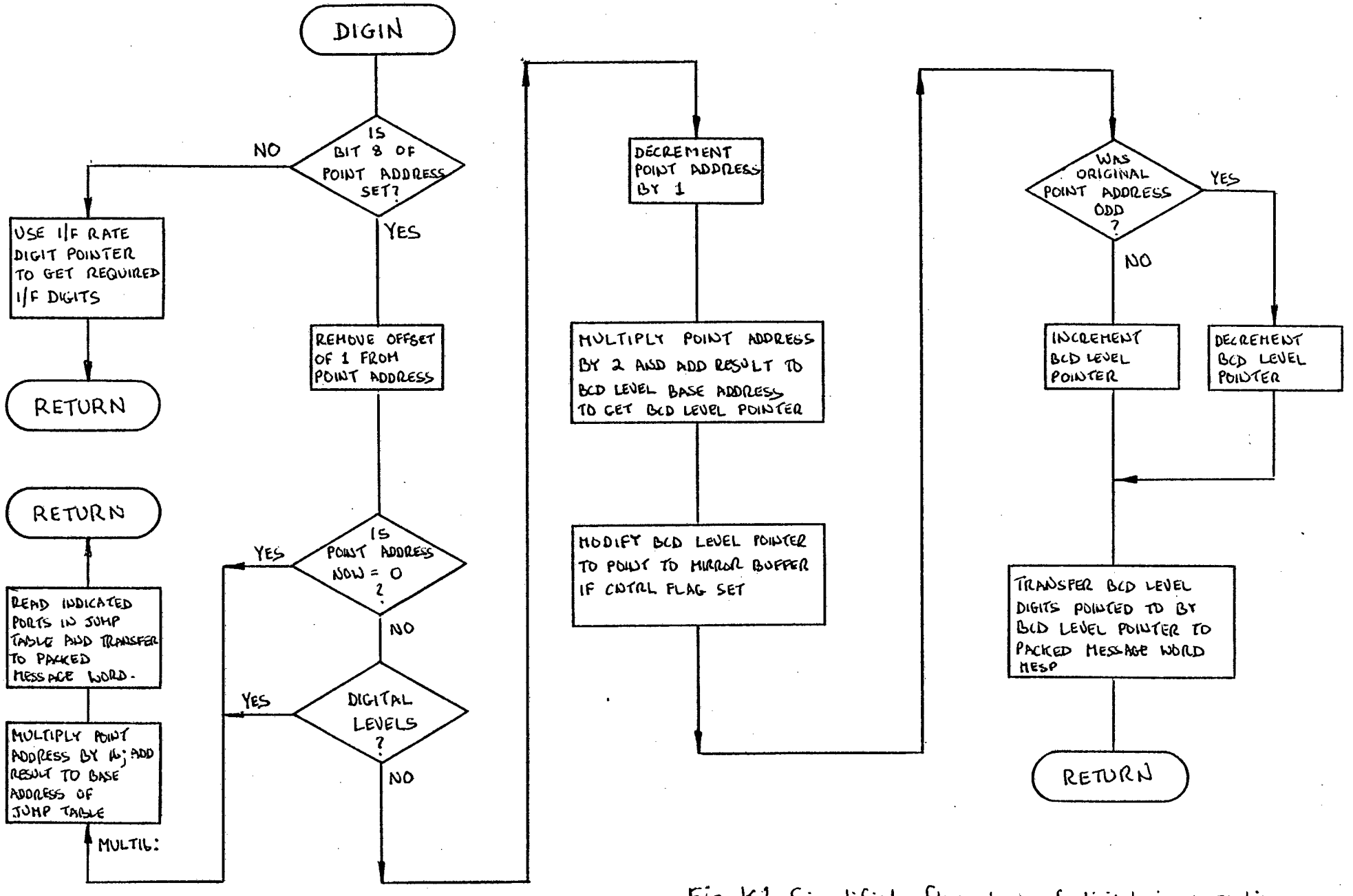


Fig K1 Simplified flow chart of digital input routine

immediately prior to this integrated flow rate request word (refer Appendix L). If bit 8 of the point address is 1 then either alarm or level information is requested; since the 4-bit sub-address referred to above (bits 9 to 12 of the request word) starts off at 1, this offset of 1 is subtracted and the result used as the basis of the alarm or level information selected.

Recall that in the Initialisation and 1 Second routines ten analogue channels are sampled ie two analogue levels and eight flow rates; the first two analogue channels provide analogue inputs for levels if required ie the new microprocessor based outstations have either analogue or digital level inputs; the choice of these two is determined by the most significant bit (bit 7) of switch bank A on the PWT board (refer paragraph 3.7.2.1) ie if it is set to 1, then these two levels are read from digital inputs, if it is clear, then these two levels are read from the first two channels of the A/D board; this is discussed in paragraph 3.2. In either case, levels are of course digital in nature and are treated as such by the software.

If the calculated point address as described above is zero, then the alarm word has been requested and the routine branches to MULT16:. DIGIN then interrogates bit 7 of switch bank A on the PWT board and if it is set, then digital levels are required and the routine branches to MULT16: where the calculated point address is multiplied by 16, added to the base address of a jump table, and programme execution resumed in the module JMPDIG (refer paragraph 4.6.5).

If bit 7 of switch bank A is not set, then analogue levels are required and the point address is first decremented by 1; thus a point address of zero corresponds with the first analogue level and then the address is multiplied by two since two bytes are required for each group of digits for a level (refer to Fig 4.3(a)); this result is stored in the BCD level pointer; the BCD buffer control flag, CNTRL, is interrogated and if set, the offset described in BACK is added to the above result so the mirror buffer is accessed while the Background Task is updating the LVLBASE buffer and vise versa (refer to DBUFF in paragraph 4.4).

The BCD level pointer manipulation which follows is necessary because the BCD level digits are stored in the conventional manner for the 8085 CPU ie least significant digits at lower address, most significant digits at higher address (refer to Fig 4.3(a)) whereas in the request word, this order is transposed ie lower point address of a level pair refers to BCD4, the most significant digit, and higher point address of a level pair refers to BCD's 0 to 3, the least significant digits (refer to Fig 1.4). Recall the original point addresses for the levels were 2 and 3 for level 1, 4 and 5 for level 2 and so on (refer to Fig 1.4); the corresponding derived BCD level pointer values are LVLBASE and LVLBASE+2 for level 1, LVLBASE+4 and LVLBASE+6 for level 2 and so on. Thus all odd original point addresses for levels which appear in request words for least significant digits of a level pair result in a derived BCD level pointer pointing at the most significant digit of that level pair and hence the pointer should be decremented; the opposite is the case for all even original point addresses of the level pairs.

The BCD level pointer now points to the required digits which are transferred to the packed message word MESP (refer paragraph 4.4).

APPENDIX L

STATUS OUTPUT ROUTINE (STOUT)

Refer to Fig L1 and Fig 4.4. This routine takes the point address of the status output double message, multiplies it by four since there are four bytes used per BCD integrated flow rate, and adds the result to IFBASE (refer to Fig 4.3(c)) and if set, the offset discussed in the Background Task is added to the above result so the mirror buffer is accessed while the Background Task is updating the IFBASE buffer and vise versa (refer to DBUFF in paragraph 4.4). The result is in the integrated flow rate digit pointer which now points to the least significant byte of the integrated flow rate in question. This is the pointer used by the digital input routine if an integrated flow rate request word follows immediately after this double message status output request word. This is the only case for an integrated flow rate MS or LS BCD digits select; refer paragraph 1.5.3.4(i) to (vi).

STOUT then determines from the sixteen bit data in the second half of the status output double message request word what is to be done concerning the selected integrated flow rate. If the LS BCD's are required then no further action is taken since the integrated flow rate digit pointer is pointing to the required LS BCD's. If the MS BCD's are required then the pointer is incremented to point to the MS BCD's (refer to Fig 4.3(c)). If it is an integrated flow rate reset command then the point address is multiplied by four (since there are four bytes for each partial sum corresponding with each integrated flow rate, refer to Appendix H), added to the base address of the partial sums so the required partial sum is now indicated; this partial sum is cleared. Finally, if the required function is a TELEPACE status output card reset request, no direct action is required since this refers to the arrangement for the mechanical flow rate integrators at the older non-microprocessor based TELEPACE outstations. This is discussed in paragraph 1.5.3.4.

In all the above four cases, a confirmation message is put into the packed message word MESP (refer paragraph 4.4) for the outstation reply word (refer paragraph 1.5.3.4).

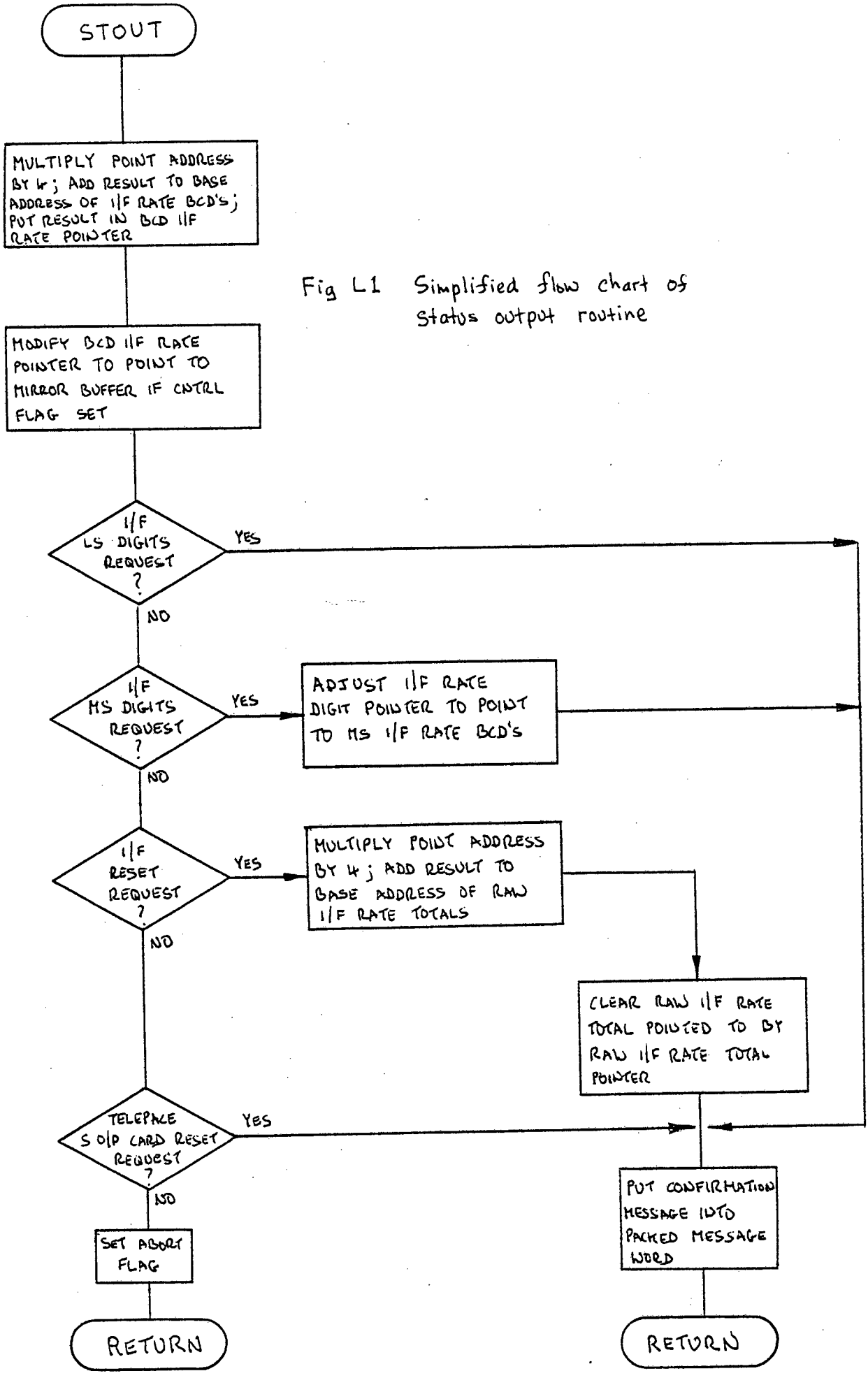


Fig L1 Simplified flow chart of status output routine

If the data in the second half of the status output double message request word is none of the above, then the abort flag FABORT is set, which is interrogated by DECODE (refer paragraph 4.6.2) and later by RX (refer to Appendix C).

APPENDIX M

ACCURACY AND RESOLUTION OF LEVEL PARAMETERS

The electromechanical level transducers decribed in paragraph 3.2 which are used for digital level input quantities provide a 5-digit BCD readout ie a resolution of 1 part in 100 000. The writer was intrigued at the excessive resolution of these transducers which obviously exceeds their accuracy which would be in the range of 1 part in 1000 ie two orders of magnitude less. As these are very old units, no information was to hand. A clue as to the motives behind the seemingly excessive resolution was found by observing the mode of operation at several dam sites. It was noticed that although the transducers have a range of 0 to 99.999 metres the dam level seldom varied by more than 10 meters or so ie they were operated over a mere 10% of their working range. It should also be borne in mind that at a large dam site, a small variation of even 10mm represents a significant amount of water. Another factor is that it is seldom necessary to know the absolute volume of water in a dam but rather the amount by which it has changed; this is obviously related to the change in level. These two factors would somewhat justify the excessive resolution as long as it is very clearly understood that comparable accuracy is by no means implied.

The writer's opinion is supported by the fact that the flow rate parameters, which are derived from analogue transducers, have a resolution of only 1 part in a 1000 ie 0.1% (refer paragraph 2.4.2.3). A comparable accuracy is readily achievable with analogue circuitry. In fact, with reference to paragraph 3.8.2.4(ii)(d), where the voltage-to-frequency converter of the A/D module is set up, it was found that tracking between frequency output and voltage input was within ten counts. Since the working range of the voltage-to-frequency converter is 0 to 10 000, this implies an accuracy of 0.1% but a resolution of 0.01% for the A/D module. Hence the accuracy of the analogue flow rate transducers and the A/D module are well matched at 0.1%.

The same A/D module is used for the analogue levels so the above discussion has an important implication when analogue level transducers are used ie a loss of the 1 part in 100 000 resolution of the digital level transducers down to the 1 part in 10 000 of the A/D module, but both with a comparable accuracy of 0.1%. To accomodate this consequential loss of resolution when analogue levels are used, the Background Task actually appends a trailing zero to the converted BCD level from the raw value obtained from the A/D board (refer Appendix I). The writer is well aware that this does not compensate for the loss of resolution, nor is it a desirable situation but unfortunately was obliged to do this due to a system constraint ie no access to the master station software.

Conversely, for the flow rates, which have always been analogue quantities, the least significant BCD digit obtained after conversion from the raw flow rate value is discarded. The accuracy and resolution of the printed result are now both 0.1%, an acceptable situation.

APPENDIX N

DATA SHEETS

The following data sheets were included because it was felt that they are not commonly used devices and are worthy of note.

1. TCM3101 SINGLE CHIP MODEM
2. DG506 16-CHANNEL ANALOGUE MUTIPLEXER
3. 6N137 LSTTL/TTL COMPATABLE OPTOCOUPLER
4. PM671 24-PIN DIP COMPATABLE DC/DC CONVERTER
5. DP8311 OCTAL LATCHED PERIPHERAL DRIVER

TCM3101 SINGLE CHIP MODEM

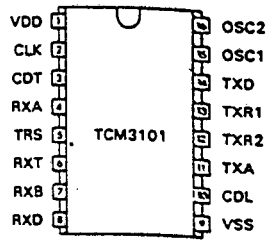
MANUFACTURER: TEXAS INSTRUMENTS

TELECOM CIRCUITS

TCM3101 SINGLE CHIP MODEM

Features

- Single chip FSK modem
- Meets CCITT V23 or Bell 202 standards
- Transmit modulation at 75, 150, 600, 1200 Baud
- Receive demodulation at 600, 1200 Baud
- Full duplex operation up to 1200 Baud recieve, 150 Baud transmit
- Half duplex operation up to 1200 Baud transmit and receive
- Carrier detect level adjustment and carrier fail output
- On chip compromize line equalization and transmit/receive filtration
- Reliable CMOS silicon gate technology
- 16 pin package



Absolute Maximum Ratings

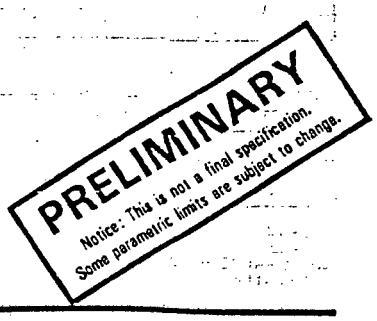
Supply Volage V_{DD} ..... −0.3-10 V
Voltage on any terminal ..... −0.3-V_{DD}
Operating free air temperature range . −10-+70°C
Storage temperature range ..... −55-+150°C

Notes :
Unless otherwise stated, all voltages are with respect to V_{SS}. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functionel operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may effect device reliebility.

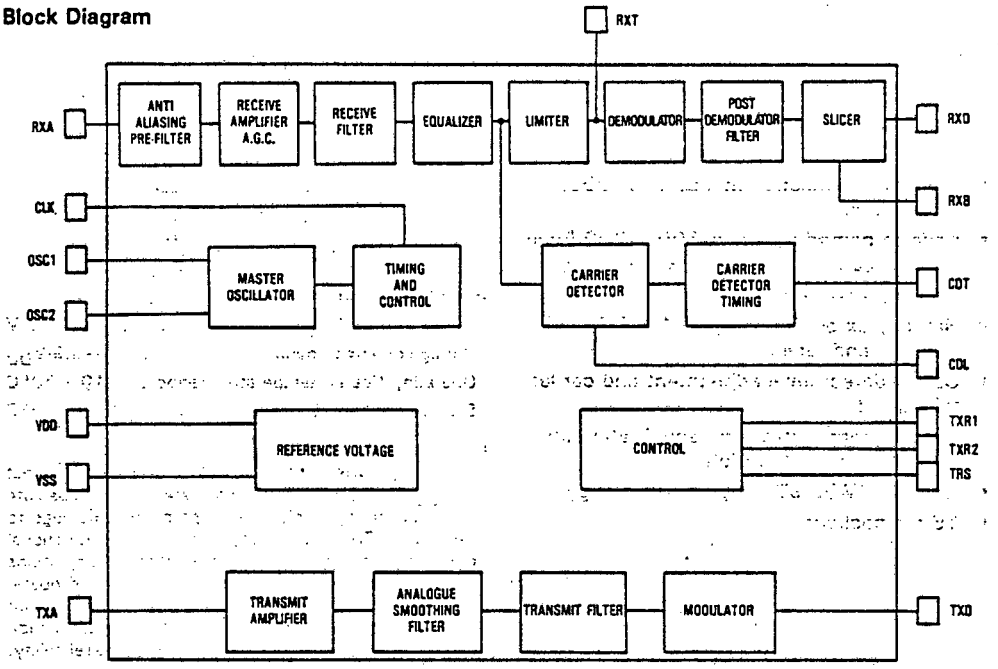
Description

The TCM3101 single chip modem is a versatile medium speed frequency shift keying (FSK) modem using silicon gate CMOS technology with switched capacitor filtering techniques. The transmitter contains a modulator which generates a pair of frequencies (selectable to CCITT V23 or Bell 202 standard frequencies by the TXR1, TXR2 and TRS inputs) representing high level and low level data inputs on the TXD input.

The receive section takes the analogue signal from the telephone line into the RXA input. This signal is normelly very distorted, can be shifted in frequency and is of variable level. A compromize line equalizer, bias distortion adjustment, carrier detect level adjustment and automatic gain control (AGC) are provided to optimize the performance and give lowest possible error rates. The carrier detect circuity sets a flag on the CDT output if the level of received inband energy falls below a value set on the CDL input, this gives carrier fail information to the system.



Block Diagram



TRANSMIT STANDARD SELECT/FREQUENCY CODE ASSIGNMENTS

TRS	STANDARD	TXR1	TXR2	TRANSMITTED BIT RATE (b/s)	TXD	TX FREQUENCY (Hz)
0 or 1	CCITT	1	0	75	1	M 390
					0	S 450
		0	1	600	1	M 1300
					0	S 1700
		0	0	1200	1	M 1300
					0	S 2100
CLK	BELL 202	1	0	150	1	M 387
					0	S 487
		0	X	1200	1	M 1200
					0	S 2200
X		1	1	0	X	Transmitter disabled

RECEIVE STANDARD SELECT

TRS	STANDARD	RECEIVED BIT RATE (b/s)	CLK FREQUENCY (KHz)
1	CCITT V23	600	9.58
0 CLK	CCITT V23 BELL 202	1200	19.11

0 = VSS
1 = VD
CLK = Connect TRS pin to CLK pin
X = Don't Care

RECOMMANDED OPERATING CONDITIONS

PARAMETERS	MIN.	TYP.	MAX.	UNIT
VDD supply voltage	4	5	6	V
Digital input levels VIH VIL	 2.0 VSS		 VDD 0.8	 V V
VRXA analog input levels (AC coupled)			0.78	V PK-PK
Master clock frequency (quartz PAL)	4.4334	4.4336	4.4338	MHz

ELECTRICAL CHARACTERISTICS

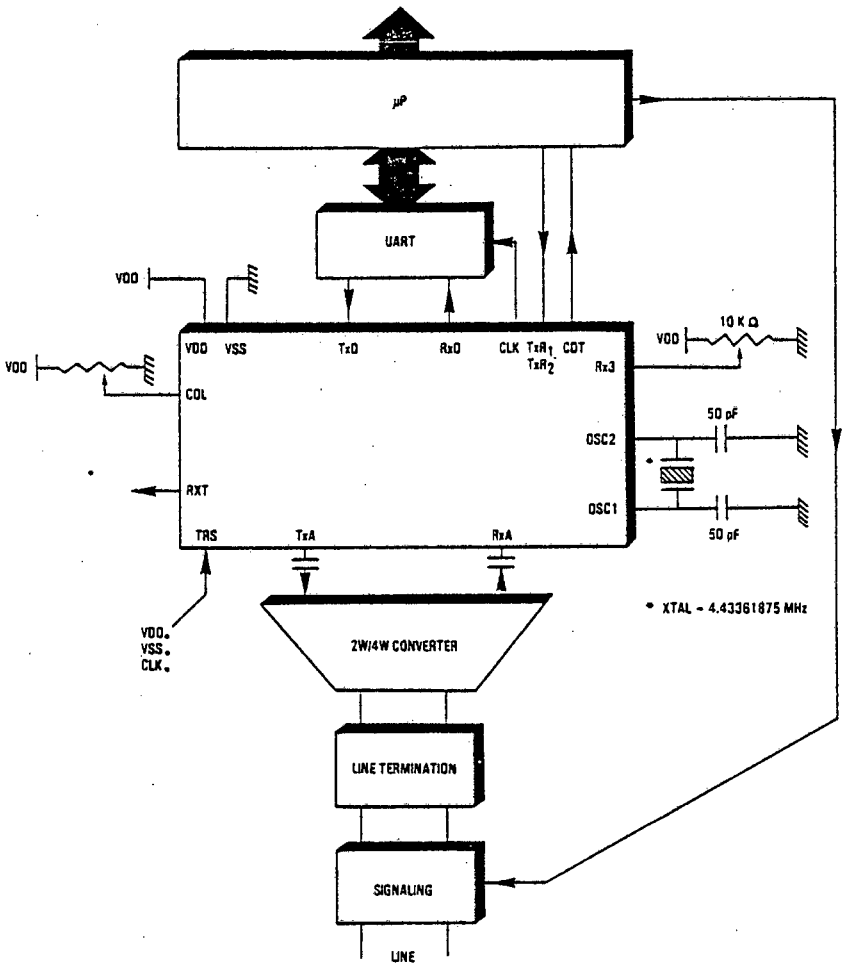
over recommended operating free-air temperature range (-10 to 70° C)

PARAMETERS	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
IDD supply current	VDD = 4 V VDD = 5 V VDD = 6 V			3.5 5.5 7.5	mA mA mA
IDD digital input current	VSS ≤ VIN ≤ VDD			±1	uA
IIA analog input current				±10	uA
Digital output level VOH VOL	 IOH ≤ 100 UA IOL ≤ 1.6 MA	 2.4 VSS		 VDD 0.4	 V V
Analog output level (see fig. 7) VTXA	VDD = 4 V VDD = 5 V VDD = 6 V RL = 50 K CL = 100 pF		1.3 1.6 1.9		V PK – PK V PK – PK V PK – PK
Analog output DC offset			VDD/2		V
Input capacitance	F = 1 MHz			15	pF
Output capacitance	F = 1 MHz			15	pF

CARRIER DETECTOR CHARACTERISTICS

PARAMETERS	MIN.	TYP.	MAX.	UNIT
Carrier detect threshold CTHH (Off-On) CTHH (On-Off) CTHH-CTHL	 -45.5 -48	 2.5	 -43 -45.4	 dBm dBm dBm
Carrier detect delay TD Off-On TD On-Off	 12 14		 19 15	 ms ms

Typical Application circuit



DG506 16-CHANNEL ANALOGUE MULTIPLEXER

MANUFACTURER: SILICONIX

EQUIVALENTS:	IH6116	(INTERSIL)
	HI506	(HARRIS)
	AD7506S	(ANALOG DEVICES)
	LF1106	(NATIONAL SEMICONDUCTOR)
	MUX16A	(PMI)

Differential 8-Channel/ 16-Channel CMOS Analog Multiplexer *designed for...*

- **Data Acquisition Systems**
- **Multiplexing Reference Signals**
- **Communication Systems**

Siliconix

BENEFITS

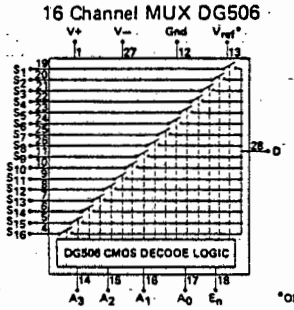
- Environmentally Rugged
  - Latchproof CMOS
- Easily Interfaced
  - TTL, DTL and CMOS Direct Control Over Military Temperature Range
- Low Stand-By Power
  - 36 mW Typical Stand-By Power
- Reduces System Cross-Talk
  - Break-Before-Make Switching Action
- Reduces External Component Requirements
  - ±15 V Analog Signal Range with ±15 V Supplies

DESCRIPTION

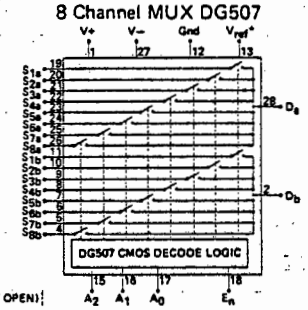
The DG506 is a single-pole 16-position (plus OFF) electronic switch array [DG507 is a double-pole 8-position (plus OFF)] which employs 16 pairs of complementary MOS (CMOS) field-effect transistors designed to function as analog switches. In the ON condition each switch will conduct current in either direction, and in the OFF condition each switch will block voltages up to 30 volts peak-to-peak. The ON-OFF state of each switch is controlled by drivers, which are in turn controlled by a 4-bit binary word (DG507 by a 3-bit binary word) input plus an Enable-Inhibit input. The truth table below shows the binary word required to select any one of the 16 switch positions, provided a positive logic "1" is present at the Enable Input. With logic "0" at the Enable input all switches will be OFF. The logic decoder and the Enable inputs will recognize voltages between 0 and 0.8 V as logic "0" voltages, and voltages between 2.4 and 15 V as logic "1" voltages. The input can thus be directly interfaced with TTL, DTL, RTL, CMOS and certain PMOS circuits. Switch action is break-before-make.

FUNCTIONAL DIAGRAMS

16 Channel MUX DG506



8 Channel MUX DG507

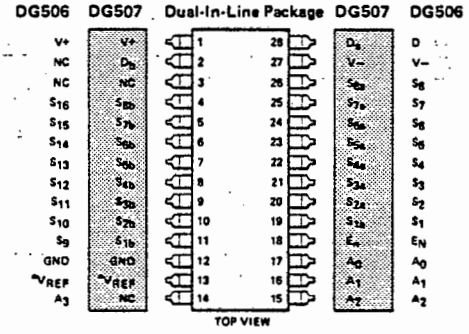


TRUTH TABLE

A_3	A_2	A_1	A_0	E_n	ON SWITCH	
X	X	X	X	0	NONE	DG507 / DG506
0	0	0	0	1	1	
0	0	0	1	1	2	
0	0	1	0	1	3	
0	0	1	1	1	4	
0	1	0	0	1	5	
0	1	0	1	1	6	
0	1	1	0	1	7	
0	1	1	1	1	8	
1	0	0	0	1	9	
1	0	0	1	1	10	
1	0	1	0	1	11	
1	0	1	1	1	12	
1	1	0	0	1	13	
1	1	0	1	1	14	
1	1	1	0	1	15	
1	1	1	1	1	16	

Logic "0" = $V_{AL} \leq 0.8V$, Logic "1" = $V_{AH} \geq 2.4$ V, Screen is DG507

PIN CONFIGURATIONS



*OPTIONAL (NORMALLY LEFT OPEN)
V+ COMMON TO SUBSTRATE

ORDER NUMBERS:

DG506AR OR DG506BR	DG506CJ
DG507AR OR DG507BR	DG507C
SEE PACKAGE 13	SEE PACKAGE 14

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En, or V_{REF}) to Ground ..... –0.3 V, V+
V_S or V_D to V+ ..... 0, –32 V
V_S or V_D to V– ..... 0, 32 V
V+ to Ground ..... 16 V
V– to Ground ..... –16 V
Current (Any Terminal, Except S or D) ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 msec, 10% Duty Cycle Max) .... 40 mA
Storage Temperature (A & B Suffix) ..... –65 to 150°C
(C Suffix) ..... –65 to 125°C
Operating Temperature (A Suffix) ..... –55 to 125°C
(B Suffix) ..... –20 to 85°C
(C Suffix) ..... 0 to 70°C
Power Dissipation (Package)*
28 Pin DIP** ..... 1200 mW
28 Pin Plastic DIP*** ..... 625 mW

*All leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C.
***Derate 8.3 mW/°C above 25°C.

"Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits."

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

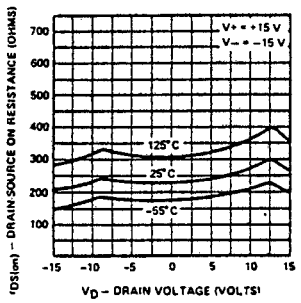
		CHARACTERISTIC		MEASURED TERMINAL	NO. TESTS PER TEMP	(Note 1) TYP 25°C	MAX LIMITS A SUFFIX –55°C	A SUFFIX 25°C	A SUFFIX 125°C	B/C SUFFIX –20/0°C	B/C SUFFIX 25°C	B/C SUFFIX 85/70°C	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V– = –15 V, Ground = 0, V_{REF} = Open (Note 4)	
1		V_{ANALOG} Minimum Analog Signal Handling Capability				±15		±15	±15		±15	±15	V	Switch ON I_S = 10 mA	
2		$r_{DS(on)}$ Drain Source ON Resistance		S to D	16	270	400	400	500	450	450	550	Ω	V_D = 10 V, I_S = –200 μA	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
3					16	230	400	400	500	450	450	550		V_D = –10 V, I_S = –200 μA	
4		$\Delta r_{DS(on)}$ Greatest Change in Drain-Source ON Resistance Between Channels		S to D	16	8							%	$\Delta r_{DS(on)} = \left(\frac{r_{DS(on)}^{MAX} - r_{DS(on)}^{MIN}}{r_{DS(on)}^{AVE}}\right)$ –10 V ≤ V_S ≤ 10 V	
5	SWITCH	$I_{S(off)}$ Source OFF Leakage Current		S	16	–0.005		±1	±50		±5	±50	nA	V_S = 10 V, V_D = –10 V	V_{EN} = 0
6					16	–0.005		±1	±50		±5	±50		V_S = –10 V, V_D = 10 V	
7		$I_{D(off)}$ Drain OFF Leakage Current	DG506	D	1	–0.03		±10	±300		±20	±300		V_D = 10 V, V_S = –10 V	
8					1	–0.03		±10	±300		±20	±300		V_D = –10 V, V_S = 10 V	
9			DG507		2	–0.015		±5	±200		±10	±200		V_D = 10 V, V_S = –10 V	
10					2	–0.015		±5	±200		±10	±200		V_D = –10 V, V_S = 10 V	
11		$I_{D(on)}$ (Note 2) Channel ON Leakage Current	DG506	D	16	–0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = 10 V	Sequence each switch on V_{AL} = 0.8 V, V_{AH} = 2.4 V
12					16	–0.06		±10	±300		±20	±300		$V_{S(all)}$ = V_D = –10 V	
13			DG507		16	–0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = 10 V	
14					16	–0.03		±5	±200		±10	±200		$V_{S(all)}$ = V_D = –10 V	
15	INPUT	I_{AH} Address Input Current, Input Voltage High		A_0, A_1, A_2, (A_3) EN	(5) 4	–0.002		–10	–30		–10	–30	μA	V_A = 2.4 V	
16					(5) 4	0.006		10	30		10	30		V_A = 15 V	
17		$I_{A(peak)}$ Peak Address Input Current			(5) 4	–75								See Curve "I_A vs V_A"	
18		I_{AL} Address Input Current, Input Voltage Low			3	–0.002		–10	–30		–10	–30		V_{EN} = 2.4 V	All V_A = 0
19					1	–0.002		–10	–30		–10	–30		V_{EN} = 0	
20	DYNAMIC	$t_{transition}$ Switching Time of Multiplexer		D		0.6		1					μs	See Figure 1	
21		t_{open} Break-Before-Make Interval		D		0.2									
22		$t_{on(EN)}$ Enable Turn-ON Time		D	1	1.0		1.5						See Figure 2	
23		$t_{off(EN)}$ Enable Turn-OFF Time		D	1	0.4		1							
24		OFF Isolation (Note 3)		D		68							dB	V_{EN} = 0, R_L = 1K Ω, C_L = 15 pF V_S = 7 VRMS, f = 500 KHz	
25		$C_{S(off)}$ Source OFF Capacitance		S	16	6							pF	V_S = 0	V_{EN} = 0, f = 140 KHz
26		$C_{D(off)}$ Drain OFF Capacitance	DG506	D	1	45								V_D = 0	
27			DG507		2	23									
28	SUPPLY	I_+ Positive Supply Current		V+	1	5.2		10				10	mA	V_{EN} = 5 V	All V_A = 0
29		I_- Negative Supply Current		V–	1	–5.2		–10				–10			
30		I_+ Positive Supply Current		V+	1	1.2		2.5				2.5		V_{EN} = 0	
31		I_- Negative Supply Current		V–	1	–1.2		–2.5				–2.5			

NOTES:
1. Typical Values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. $I_{D(on)}$ is leakage from driver into "ON" switch.
3. OFF Isolation $\triangleq 20 \log \frac{|V_O|}{|V_S|}$ V_S = input to "OFF" switch V_O = output due to V_S.
4. Functional operation is possible for supply voltages less than 15 V, but the input logic threshold will shift. For V+ = |V–| < 10 V, 1.5 V may be applied to the V_{REF} terminal. The V_{REF} terminal has R_{IN} ≥ 45K Ω (See the applications section.)

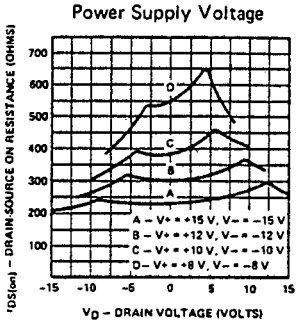
DG506 ICX8A.
DG507 ICX8B

TYPICAL CHARACTERISTICS

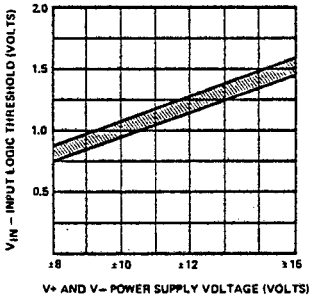
$r_{DS(on)}$ vs V_D and Temperature



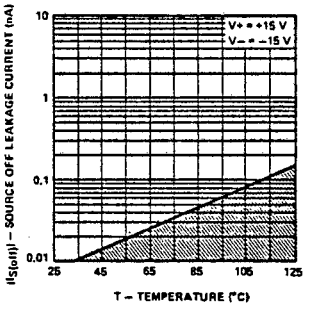
$r_{DS(on)}$ vs V_D and Power Supply Voltage



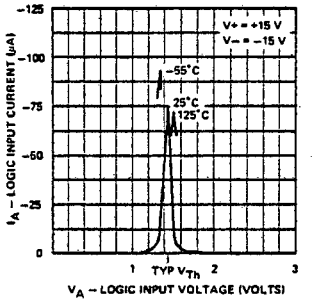
Logic Threshold vs Power Supply Voltage



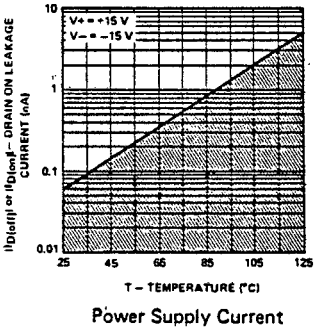
$I_{S(off)}$ vs Temperature*



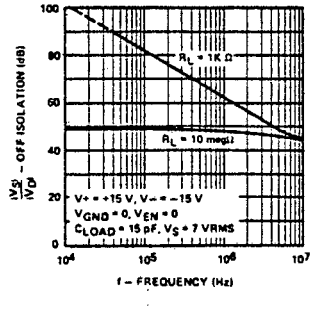
I_A vs V_A (Terminals A_0, A_1, A_2, A_3, EN)



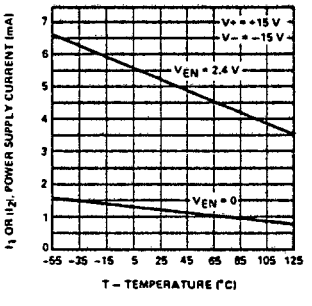
$I_{D(off)}$ and $I_{D(on)}$ vs Temperature*



OFF Isolation vs Frequency

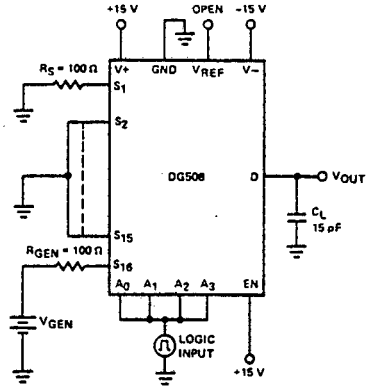


Power Supply Current vs Temperature

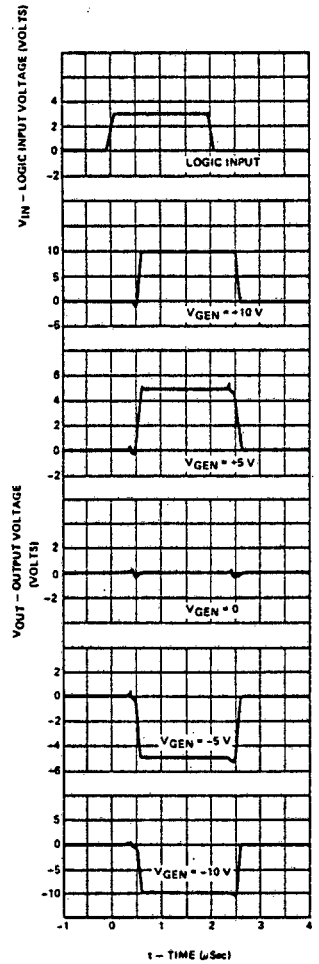


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

Typical delay, rise, fall, settling times, and switching transients in this circuits.

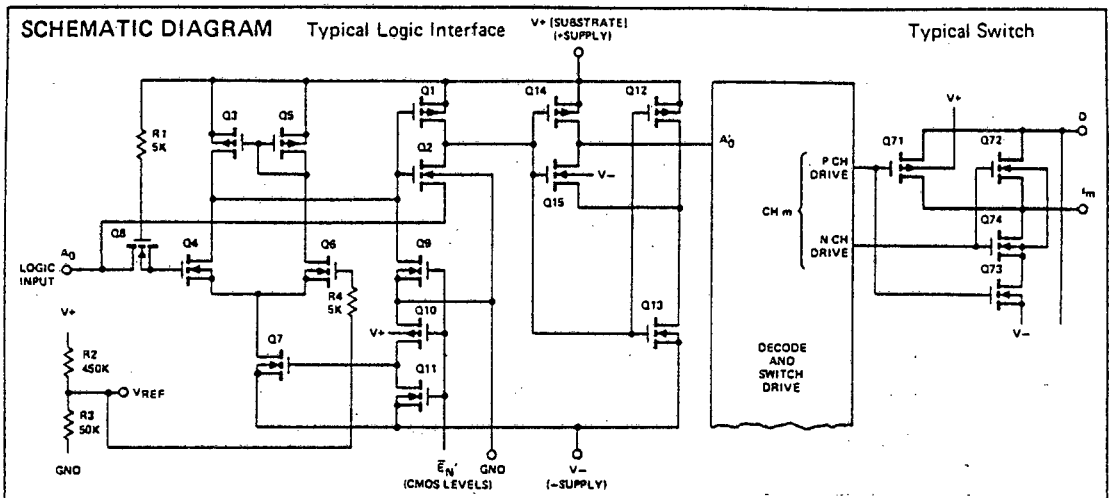


If R_{GEN}, R_S, or C_L is increased, there will be proportional increases in rise and/or fall RC times.

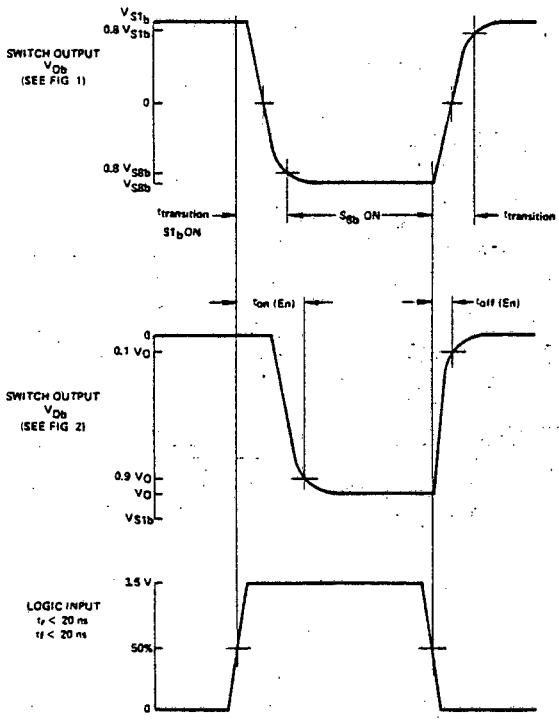


SCHEMATIC DIAGRAM

Typical Logic Interface



SWITCHING TIME TEST CIRCUIT



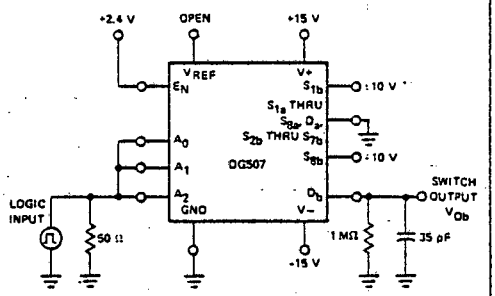


Figure 1

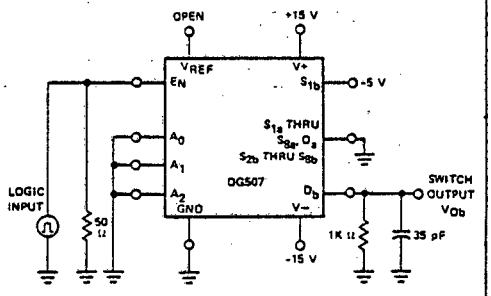


Figure 2

APPLICATIONS

Application Hints*

V+ Positive Supply Voltage (V)	V– Negative Supply Voltage (V)	V_{REF} Reference Pin Connection (V)	V_{IN} Logic Input Voltage V_{INH} Min/ V_{INL} Max (V)	V_S or V_D Analog Voltage Range (V)
+15**	–15	Open	2.4/0.8	–15 to +15
+12	–12	Open or 1.4 V	2.4/0.8	–12 to +12
+10	–10	1.4 V	2.4/0.8	–10 to +10
+8***	–8	1.4 V	2.4/0.8	–8 to +8

*Application Hints are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

**Electrical Characteristics chart based on V+ = +15 V, V– = –15 V, V_{REF} = Open.

***Operation below ±8 V is not recommended.

Siliconix

6N137 LSTTL/TTL COMPATABLE OPTOCOUPLER

MANUFACTURER: HEWLETT PACKARD

HEWLETT PACKARD

LSTTL/TTL COMPATIBLE OPTOCOUPLER

6N137

TECHNICAL DATA MARCH 1980

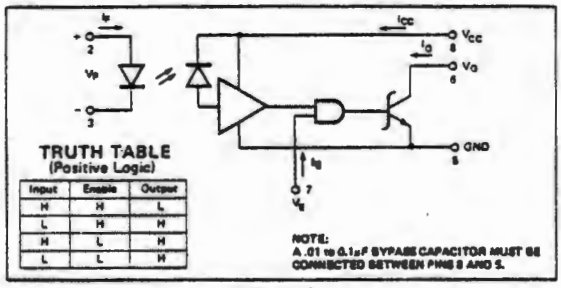


Figure 1.

Features

- LSTTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- 3000 Vdc WITHSTAND TEST VOLTAGE

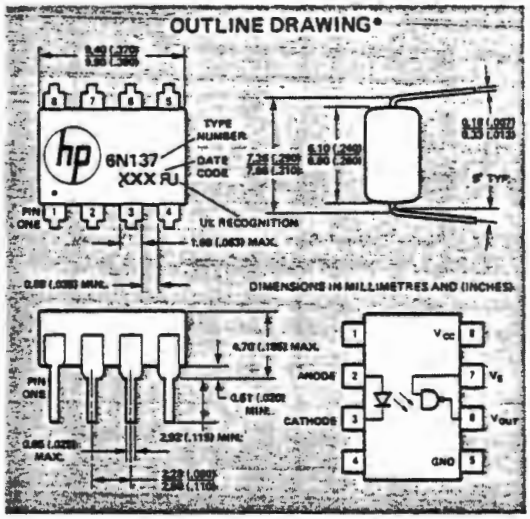
Description Applications

The 6N137 consists of a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. The circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5mA will sink an eight gate fan-out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45ns. The enable input provides gating of the detector with input sinking and sourcing requirements compatible with LSTTL/TTL interfacing and a propagation delay of 25ns typical.

The 6N137 can be used in high speed digital interfacing applications where common mode signals must be rejected, such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished in system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, OR'ing and strobing.



Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3**	15	mA
High Level Enable Voltage	V_{EH}	2.0	V_{CC}	V
Low Level Enable Voltage (Output High)	V_{EL}	0	0.8	V
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load)	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings*

(No derating required up to 70°C)

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Solder Temperature ..... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current ..... 40mA (1≤ 1msec Duration)
Average Forward Input Current 20mA
Reverse Input Voltage 5V
Enable Input Voltage ..... 5.5V (Not to exceed V_{CC} by more than 500mV)
Supply Voltage - V_{CC} ..... 7V (1 Minute Maximum)
Output Current - I_O 50mA
Output Collector Power Dissipation 85mW
Output Voltage - V_O 7V

**6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

*JEDEC Registered Data.

Electrical Characteristics

OVER RECOMMENDED TEMPERATURE (T_A = 0°C TO 70°C) UNLESS OTHERWISE NOTED

Parameter	Symbol	Min.	Typ.**	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	I_{OH}*		50	250	μA	V_{CC}=5.5V, V_O=5.5V, I_F=250μA, V_E=2.0V	6	
Low Level Output Voltage	V_{OL}*		0.5	0.6	V	V_{CC}=5.5V, I_F=5mA, V_{EH}=2.0V, I_{OL} (Sinking) =13mA	3,5	
High Level Enable Current	I_{EH}		-1.0		mA	V_{CC}=5.5V, V_E=2.0V		
Low Level Enable Current	I_{EL}*		-1.6	-2.0	mA	V_{CC}=5.5V, V_E=0.5V		
High Level Supply Current	I_{CCH}*		7	15	mA	V_{CC}=5.5V, I_F=0, V_E=0.5V		
Low Level Supply	I_{CCL}*		13	18	mA	V_{CC}=5.5V, I_F=10mA, V_E=0.5V		
Input-Output Insulation Leakage Current	I_{I-O}*			1.0	μA	Relative Humidity=45%, T_A=25°C, t=5s, V_{I-O}=3000Vdc		5
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	V_{I-O}=500V, T_A=25°C		5
Capacitance (Input-Output)	C_{I-O}		0.6		pF	f=1MHz, T_A=25°C		5
Input Forward Voltage	V_F*		1.5	1.75	V	I_F=10mA, T_A=25°C	4	8
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R=10μA, T_A=25°C		
Input Capacitance	C_{IN}		60		pF	V_F=0, f=1MHz		
Current Transfer Ratio	CTR		700		%	I_F=5.0mA, R_L=100Ω	2	7

**All typical values are at V_{CC} = 5V, T_A = 25°C

Switching Characteristics at T_A=25°C, V_{CC}=5V

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to High Output Level	t_{PLH}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	1
Propagation Delay Time to Low Output Level	t_{PHL}*		45	75	ns	R_L=350Ω, C_L=15pF, I_F=7.5mA	7,9	2
Output Rise-Fall Time (10-90%)	t_r, t_f		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA		
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}		25		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	3
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		15		ns	R_L=350Ω, C_L=15pF, I_F=7.5mA, V_{EH}=3.0V, V_{EL}=0.5V	8	4
Common Mode Transient Immunity at Logic High Output Level	CM_H		50		v/μs	V_{CM}=10V, R_L=350Ω, V_O(min.)=2V, I_F=0mA	11	6
Common Mode Transient Immunity at Logic Low Output Level	CM_L		-150		v/μs	V_{CM}=10V, R_L=350Ω, V_O(max.)=0.8V, I_F=5mA	11	6

*JEDEC Registered Data.

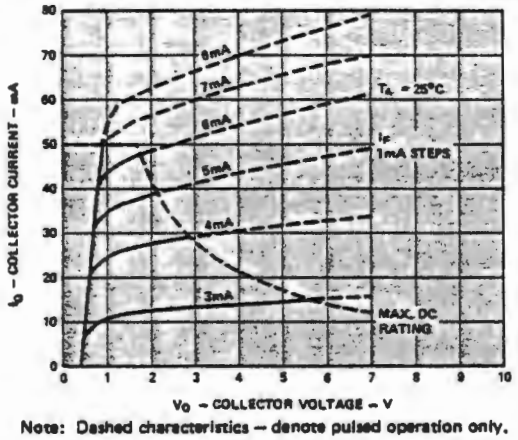
Operating Procedures and Definitions

Logic Convention. The 6N137 is defined in terms of positive logic.

Bypassing. A ceramic capacitor (.01 to 0.1μF) should be connected from pin 8 to pin 5 (Figure 12). Its purpose is to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching properties. The total lead length between capacitor and coupler should not exceed 20mm.

Polarities. All voltages are referenced to network ground (pin 5). Current flowing toward a terminal is considered positive.

Enable Input. No external pull-up required for a logic (1), i.e., can be open circuit.



Note: Dashed characteristics — denote pulsed operation only.

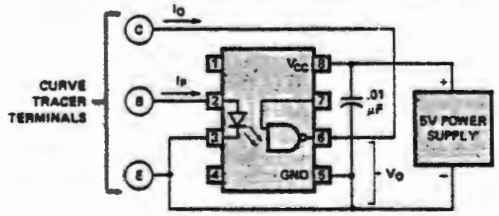
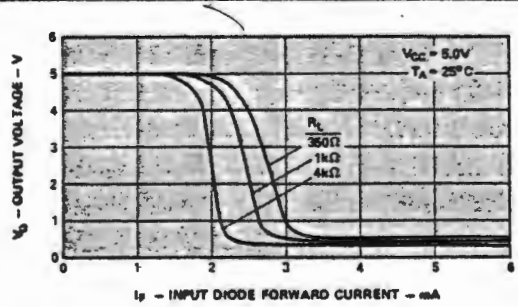


Figure 2. Optocoupler Collector Characteristics.



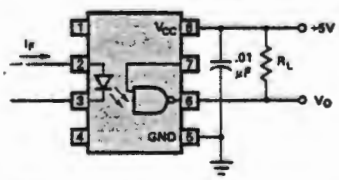


Figure 3. Input-Output Characteristics.

NOTES:

1. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
2. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to 1.5V point on the leading edge of the output pulse.
3. The t_{ELH} enable propagation delay is measured from the 1.5V point of the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
4. The t_{EHL} enable propagation delay is measured from the 1.5V point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
5. Device considered a two terminal device: pins 2 and 3 shorted together, and pins 5, 6, 7, and 8 shorted together.
6. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O>2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O<0.8V).
7. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.
8. At 10mA V_F decreases with increasing temperature at the rate of 1.6mV/°C.

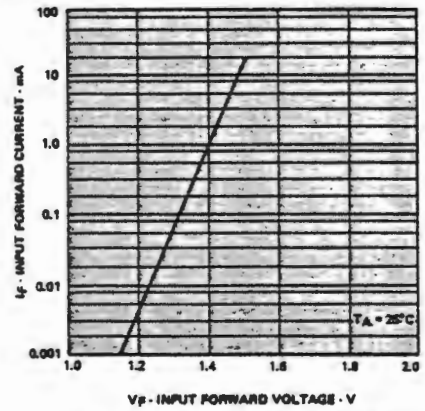


Figure 4. Input Diode Forward Characteristic.

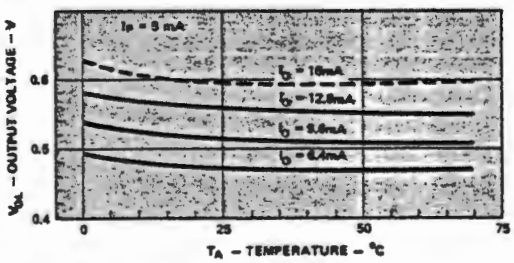


Figure 5. Output Voltage, V_{OL} vs. Temperature and Fan-Out.

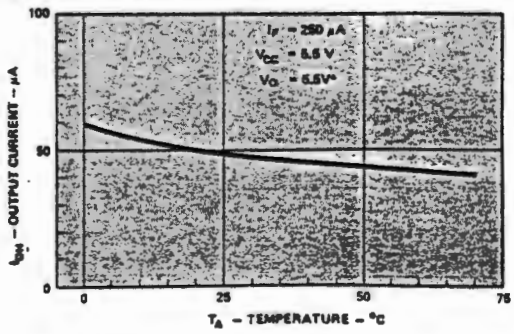


Figure 6. Output Current, I_{OH} vs. Temperature (I_F=250μA).

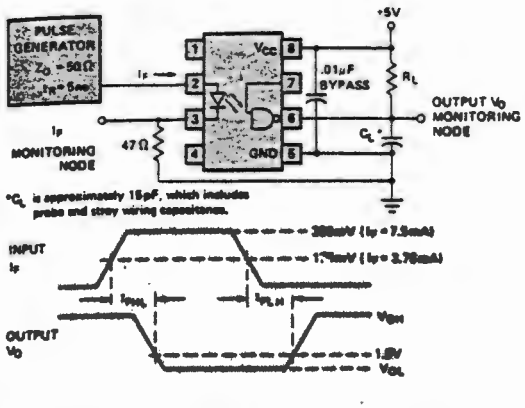


Figure 7. Test Circuit for t_{PHL} and t_{PLH}.**

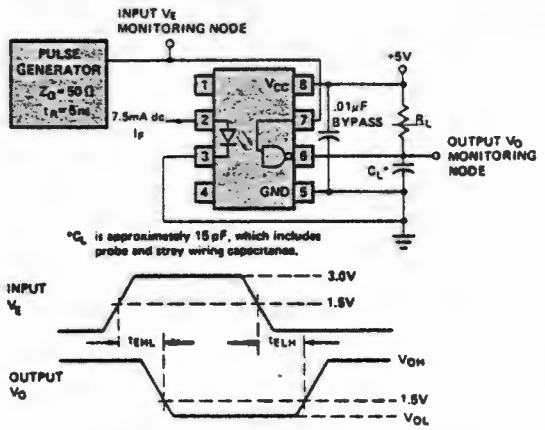


Figure 8. Test Circuit for t_{ELH} and t_{EHL}.

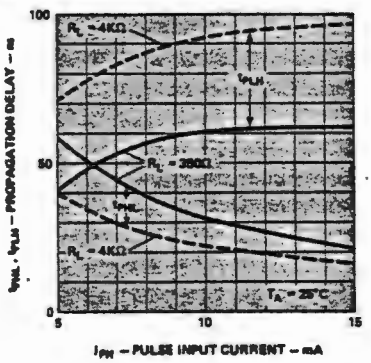


Figure 9. Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}.

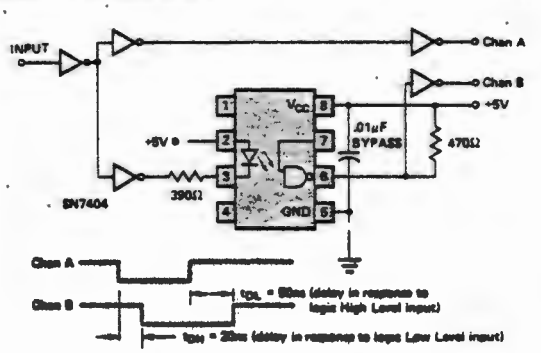


Figure 10. Response Delay Between TTL Gates.

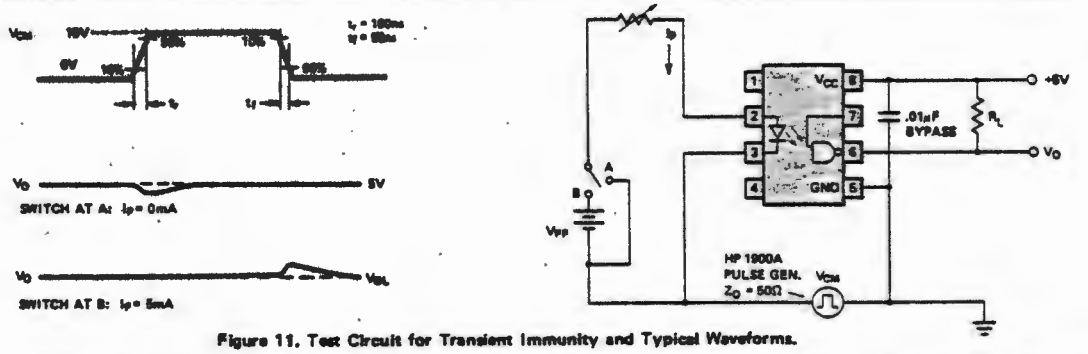


Figure 11. Test Circuit for Transient Immunity and Typical Waveforms.

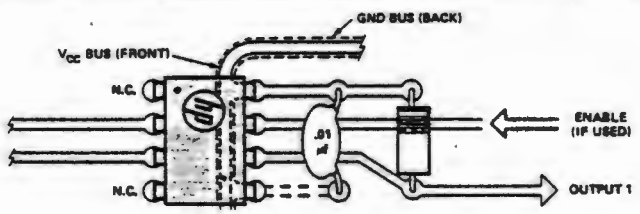


Figure 12. Recommended Printed Circuit Board Layout.

** JEDEC Registered Data.

PM671 24-PIN DIP COMPATABLE DC/DC CONVERTER

MANUFACTURER: POWER PRODUCTS

24 Pin DIP Compatible DC/DC Converters

Electrical Specifications

Input Performance
Input Current:
Full Load...Output Power/Input Voltage x Efficiency
No Load...30% (Max.) of Full Load Input Current
Fault Mode Current:
150% (Max.) of Full Load Input Current
Reflected Ripple Current:
5VDC Input, Filtered...15mA, Peak-to-Peak
12VDC Input, Filtered...45mA, Peak-to-Peak
All Models, Unfiltered...1500mA, Peak-to-Peak

Output Performance
Line Regulation:
±0.3%, Low Line to High Line
Load Regulation:
±0.4%, No Load to Full Load
Output Voltage Accuracy:
±5%, Fixed
Balance (Dual Output Models Only):
±5%
Temperature Coefficient:
±.01%/°C, Typical
Warm-Up Drift:
±0.2%
Over Shoot:
±0.1%, 10% to 90% Load, Typical
Ripple and Noise
20mV Peak-to-Peak (With 1.5μf Tantalum Capacitor Across Each Output)
Short Circuit Protection:
Output Thermal Limited
Short Circuit Restart:
Automatic When Short Circuit is Removed

Input/Output Performance
Breakdown Voltage:
300VDC
Isolation Resistance:
10^9 Ohms, Typical
Isolation Capacitance:
80 μf, Typical
Efficiency:
50%, Typical

Power Requirements
Input Voltage Range:
5VDC Input Models...4.5VDC to 5.5VDC
12VDC Input Models...10.8VDC to 13.2VDC
Operating Frequency:
40KHz to 70KHz

Environmental Requirements
Temperature Range:
Operating Range...–25°C to +71°C (No Derating)
Storage Range...–40°C to +100°C
Humidity:
20% to 80% R.H. (Non-Condensing)

PIN CONNECTIONS

Single Output Models
+V Input 1,24
–V Input 12,13
+V Output 11,14
–V Output 10,15

Dual Output Models
+V Input 1,24
–V Input 12,13
+V Output 11,14
–V Output 2,23
Common 3,10,22,15
Balance (Optional) 9

Alternate Pin Configuration
+V Input 1,2,3
–V Input 22,23,24
+V Output 15
–V Output 13
Common 10,11
Balance 14
No Connection 12

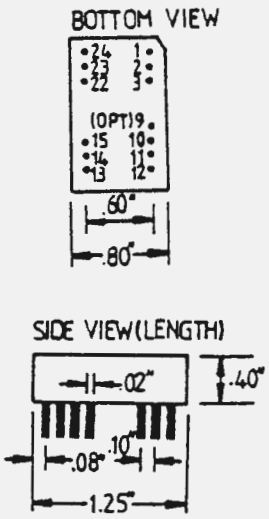
ORDERING INFORMATION

DESCRIPTION			FILTERED	UNFILTERED	ALTERNATIVE
INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT	MODEL NUMBER	MODEL NUMBER	MODEL NUMBER
5VDC	5VDC	100mA	PM621	PM641	PM601
5VDC	12VDC	80mA	PM623	PM643	PM603
5VDC	15VDC	65mA	PM624	PM644	PM604
5VDC	±12VDC	±40mA	PM671	PM691	PM651
5VDC	±15VDC	±33mA	PM672	PM692	PM652
12VDC	5VDC	100mA	PM631	PM646	PM611
12VDC	12VDC	80mA	PM633	PM648	PM613
12VDC	15VDC	65mA	PM634	PM649	PM614
12VDC	±12VDC	±40mA	PM681	PM696	PM661
12VDC	±15VDC	±33mA	PM682	PM697	PM662

OPTIONS (DUAL OUTPUT MODELS ONLY):

External Balance Pin
for output voltage adjustment or equalization. Add suffix "P" to model number.

Alternate Pin Configuration
including external balance pin. Add suffix "R" to model number.



DP8311 OCTAL LATCHED PERIPHERAL DRIVER

MANUFACTURER: NATIONAL SEMICONDUCTOR

National Semiconductor

Peripheral/Power Drivers

DP7310/DP8310/DP7311/DP8311 Octal Latched Peripheral Drivers

General Description

The DP7310/8310, DP7311/8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30 volts. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP7310/8310 are positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP7311/8311 are fall through latches. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

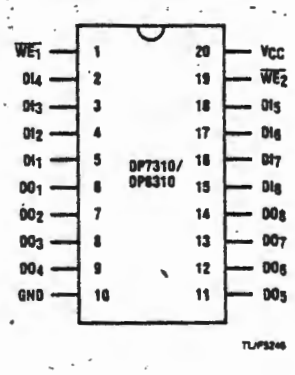
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature.
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

Connection Diagrams

Dual-In-Line Package



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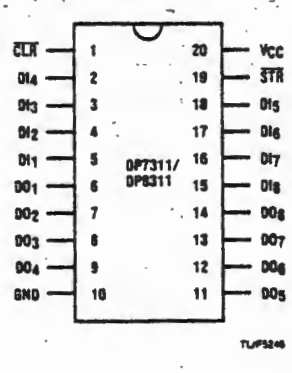
Dual-In-Line Package



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Order Number DP7310J, DP7311J, DP8310J, DP8311J, DP8310N or DP8311N
See NS Package J20A or N20A

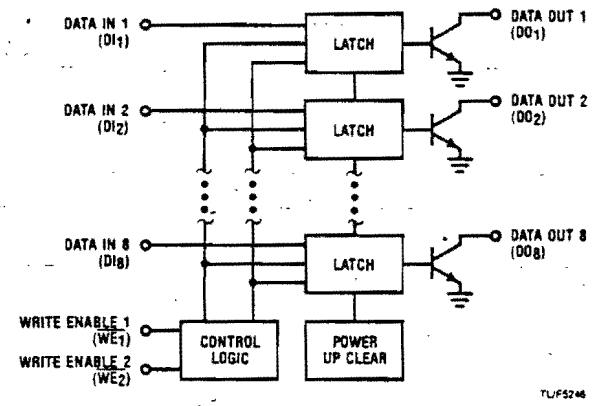
Logic Table

DP7310/DP8310			
Write Enable 1 $\overline{WE_1}$	Write Enable 2 $\overline{WE_2}$	Data Input DI_{1-8}	Data Output DO_{1-8}
0	0	X	Q
0	↓	0	1
0	↓	1	0
↓	0	0	1
↓	0	1	0
0	1	X	Q
1	0	X	Q
1	1	X	Q

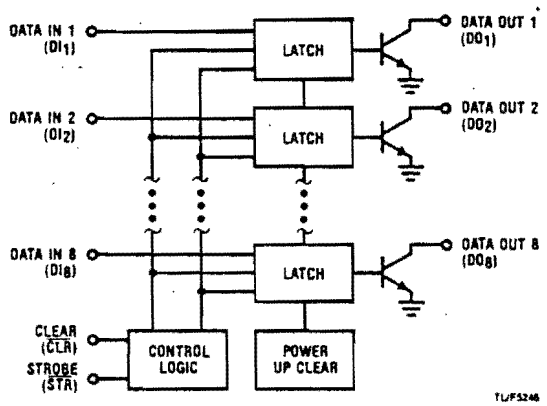
DP7311/DP8311			
Clear $\overline{CLR}$	Strobe $\overline{STR}$	Data Input DI_{1-8}	Data Output DO_{1-8}
1	1	X	Q
1	0	0	1
1	0	1	0
0	X	X	1

X = Don't Care
1 = Outputs Off
0 = Outputs On
Q = Pre-existing Output
↓ = Positive Edge Transition

Block Diagram DP7310/DP8310



Block Diagram DP7311/DP8311



Absolute Maximum Ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	35V
Output Voltage	35V
Maximum Power Dissipation* at 25°C	
Cavity Package	1821 mW
Molded Package	2005 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

*Derate cavity package 12.1 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min.	Max.	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature			
DP7310/DP7311	−55	+125	°C
DP8310/DP8311	0	+70	°C
Input Voltage		30	V
Output Voltage		30	V

DC Electrical Characteristics DP7310/DP8310, DP7311/DP8311 (Notes 2 and 3)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Logical "1" Input Voltage		2.0			V
V_{IL}	Logical "0" Input Voltage				0.8	V
V_{OL}	Logical "0" Output Voltage	Data outputs latched to logical "0", V_{CC} = min.				
	DP7310/DP7311	I_{OL} = 75 ma			0.4	V
	DP8310/DP8311	I_{OL} = 100 mA		0.35	0.5	V
I_{OH}	Logical "1" Output Current	Data outputs latched to logical "1", V_{CC} = min.				
	DP7310/DP7311	V_{OH} = 25V			500	μA
	DP8310/DP8311	V_{OH} = 30V		2.5	250	μA
I_{IH}	Logical "1" Input Current	V_{IH} = 2.7V, V_{CC} = max.		0.1	25	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 30V, V_{CC} = max.		1	250	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, V_{CC} = max.		−215	−300	μA
V_{clamp}	Input Clamp Voltage	I_{IN} = −12 mA		−0.8	−1.5	V
I_{CC0}	Supply Current, Outputs On	Data outputs latched to a logical "0". All inputs are at logical "1", V_{CC} = max.				
	DP7310			100	125	mA
	DP8310			100	152	mA
	DP7311			88	117	mA
	DP8311			88	125	mA
I_{CC1}	Supply Current, Outputs Off	Data outputs latched to a logic "1". Other conditions same as I_{CC0}.				
	DP7310			40	47	mA
	DP8310			40	57	mA
	DP7311			25	34	mA
	DP8311			25	36	mA

AC Electrical Characteristics DP7310/DP8310: $V_{CC} = 4.5V$, $T_A = -55°C$ to $125°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Write Enable Input to Output	Figure 1		40	120	ns
t_{pd1}	Low to High Propagation Delay Write Enable Input to Output	Figure 1		70	150	ns
t_{SETUP}	Minimum Set-Up Time Data In to Write Enable Input	$t_{HOLD} = 0$ ns Figure 1	45	20		ns
t_{pWH}, t_{pWL}	Minimum Write Enable Pulse Width	Figure 1	60	25		ns
t_{THL}	High to Low Output Transition Time	Figure 1		16	35	ns
t_{TLH}	Low to High Output Transition Time	Figure 1		38	70	ns
C_{IN}	"N" Package Note 4			5	15	pF

AC Electrical Characteristics DP7311/DP8311: $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd0}	High to Low Propagation Delay Data In to Output	Figure 2		30	60	ns
t_{pd1}	Low to High Propagation Delay Data In to Output	Figure 2		70	100	ns
t_{SETUP}	Minimum Set-Up Time Data In to Strobe Input	$t_{HOLD} = 0$ ns Figure 2	0	−25		ns
t_{pWL}	Minimum Strobe Enable Pulse Width	Figure 2	60	35		ns
t_{pdC}	Propagation Delay Clear to Data Output	Figure 2		70	135	ns
t_{pWC}	Minimum Clear Input Pulse Width	Figure 2	60	25		ns
t_{THL}	High to Low Output Transition Time	Figure 2		20	35	ns
t_{TLH}	Low to High Output Transition Time	Figure 2		38	60	ns
C_{IN}	Input Capacitance — Any Input	Note 4		5	15	pF

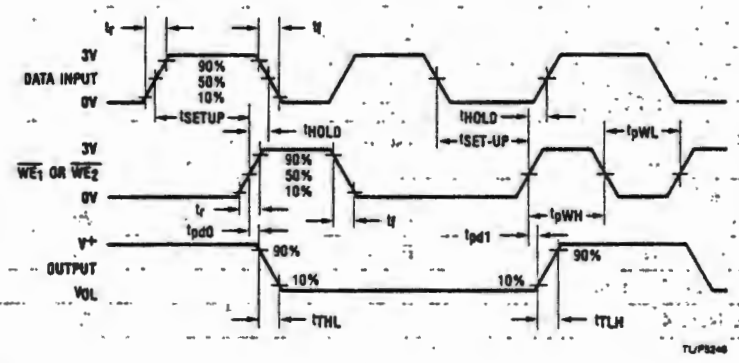
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min./max. limits apply across the −55°C to +125°C temperature range for the DP7310/DP7311 and across the 0°C to +70°C for the DP8310/DP8311. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$.

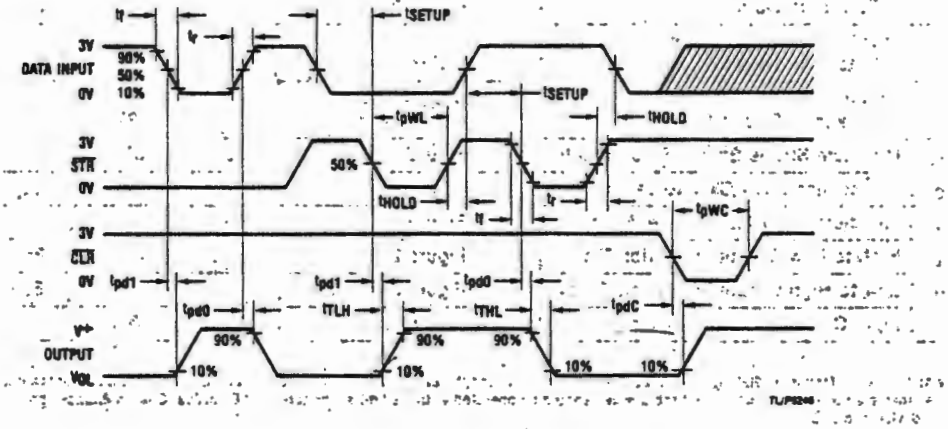
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Input capacitance is guaranteed by periodic testing. $f_{TEST} = 10$ kHz at 300 mV, $T_A = 25°C$

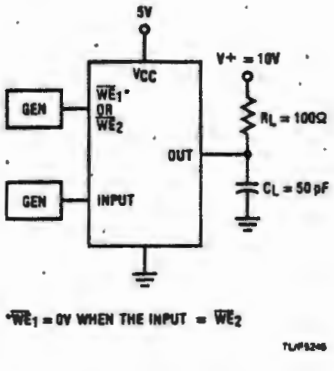
Switching Time Waveform DP7310/DP8310



Switching Time Waveform DP7311/DP8311



Switching Time Test Circuits DP7310/DP8310 DP7311/DP8311



*WE1 = 0V WHEN THE INPUT = WE2

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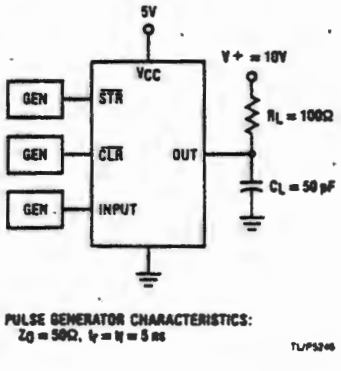
FIGURE 1



PULSE GENERATOR CHARACTERISTICS:
ZO = 50Ω, tr = tf = 5 ns

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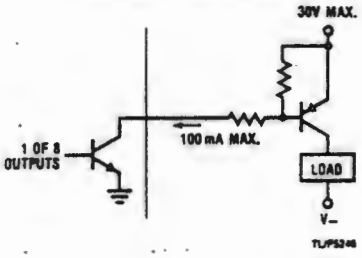
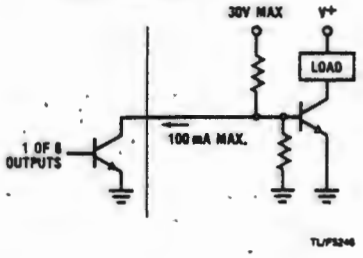
FIGURE 2

Typical Applications DP8310/11 Buffering High Current Device (Notes 1 and 2)

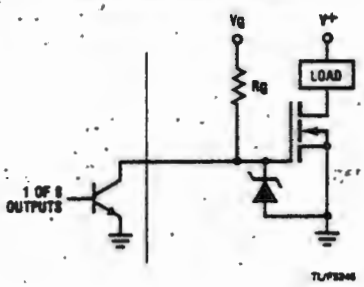
PNP High Current Driver



NPN High Current Driver

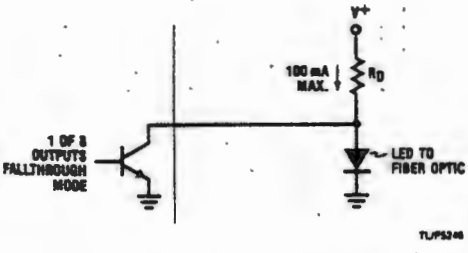


VMOS High Current Driver

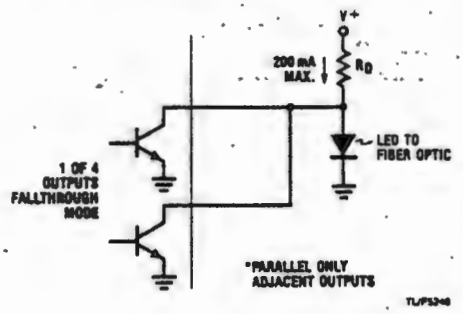


Eight Output/Four Output Fiber Optic LED Driver

DP8311 100 mA Drivers

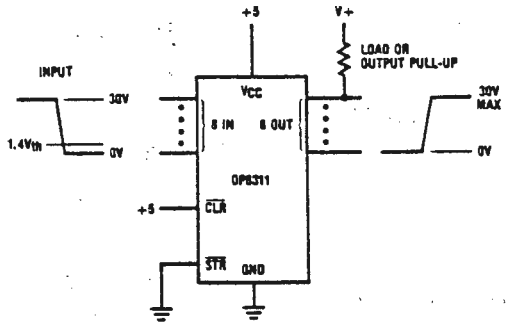


DP8311 Parallel Outputs (200 mA) Drivers*

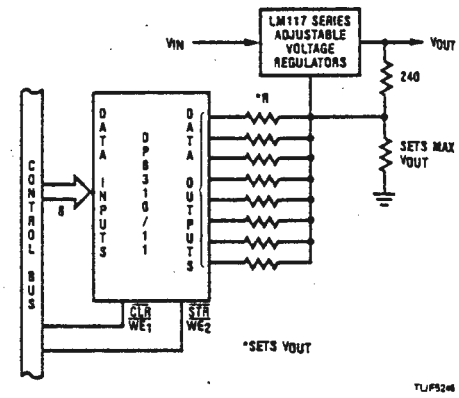


Typical Applications (cont'd)

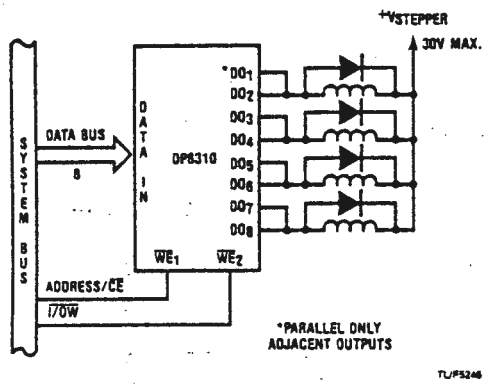
8-Bit Level Translator-Driver



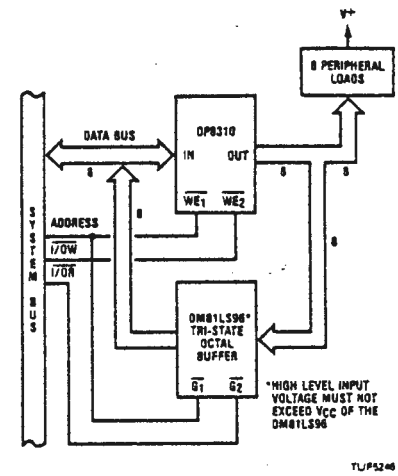
Digital Controlled 256 Level Power Supply from 1.2 Volts to 30 Volts



200 mA Drive for a 4 Phase Bifilar Stepper Motor



Reading the State of the Latched Peripherals



Note 1: Always use good V_{CC} bypass and ground techniques to suppress transients caused by peripheral loads.

Note 2: Printed circuit board mounting is required if these devices are operated at maximum rated temperature and current (all outputs on DC).